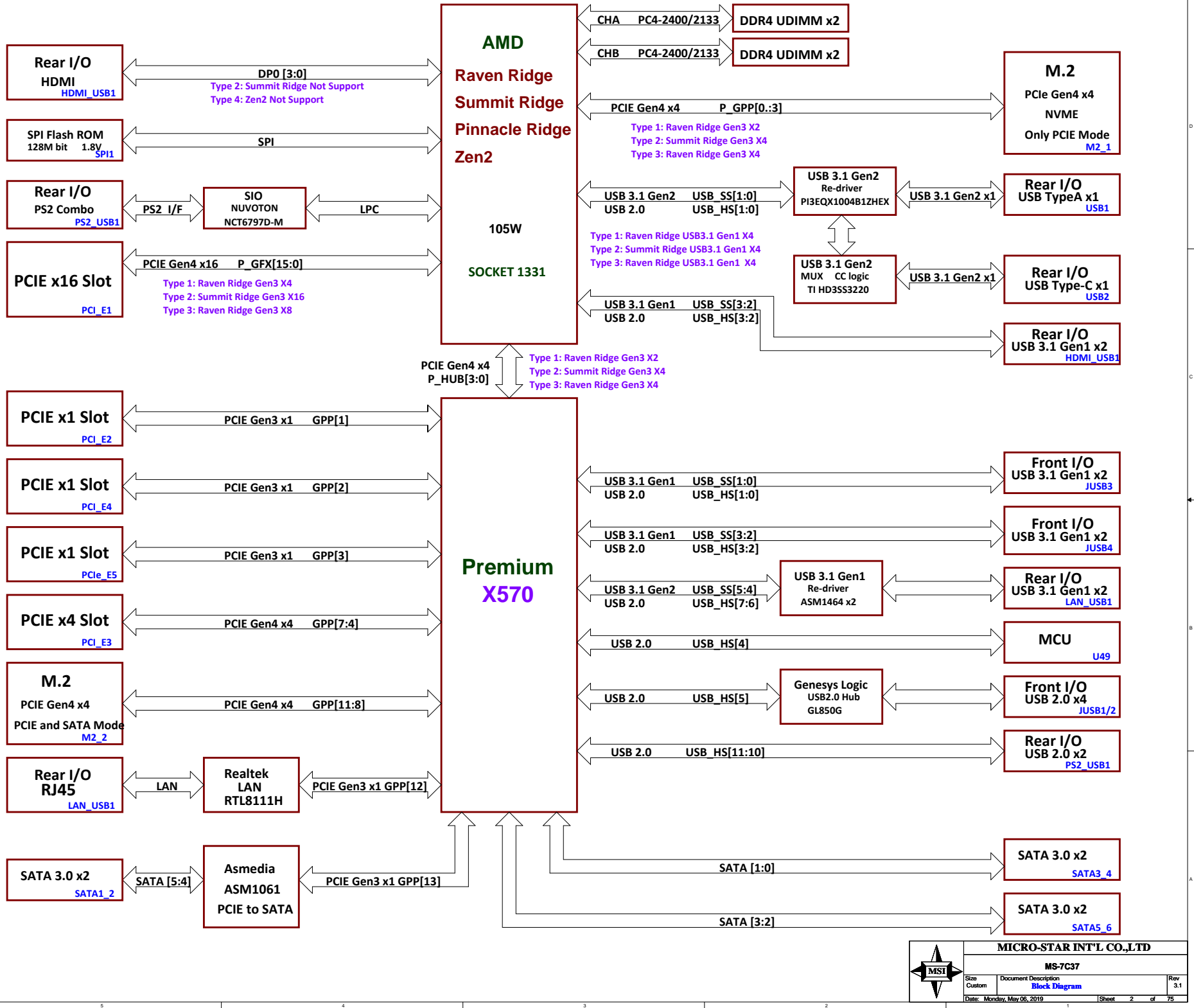
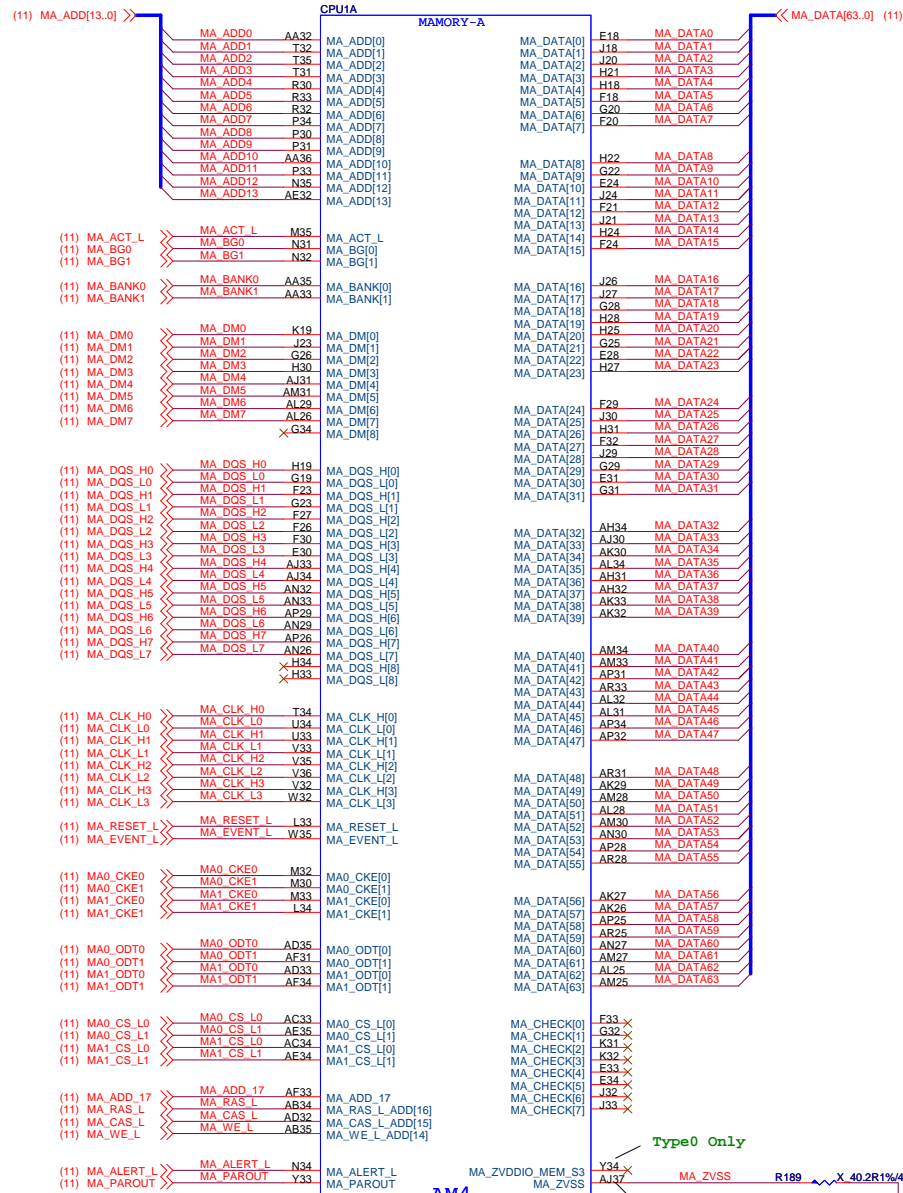


AMD AM4

GAMING EDGE AC

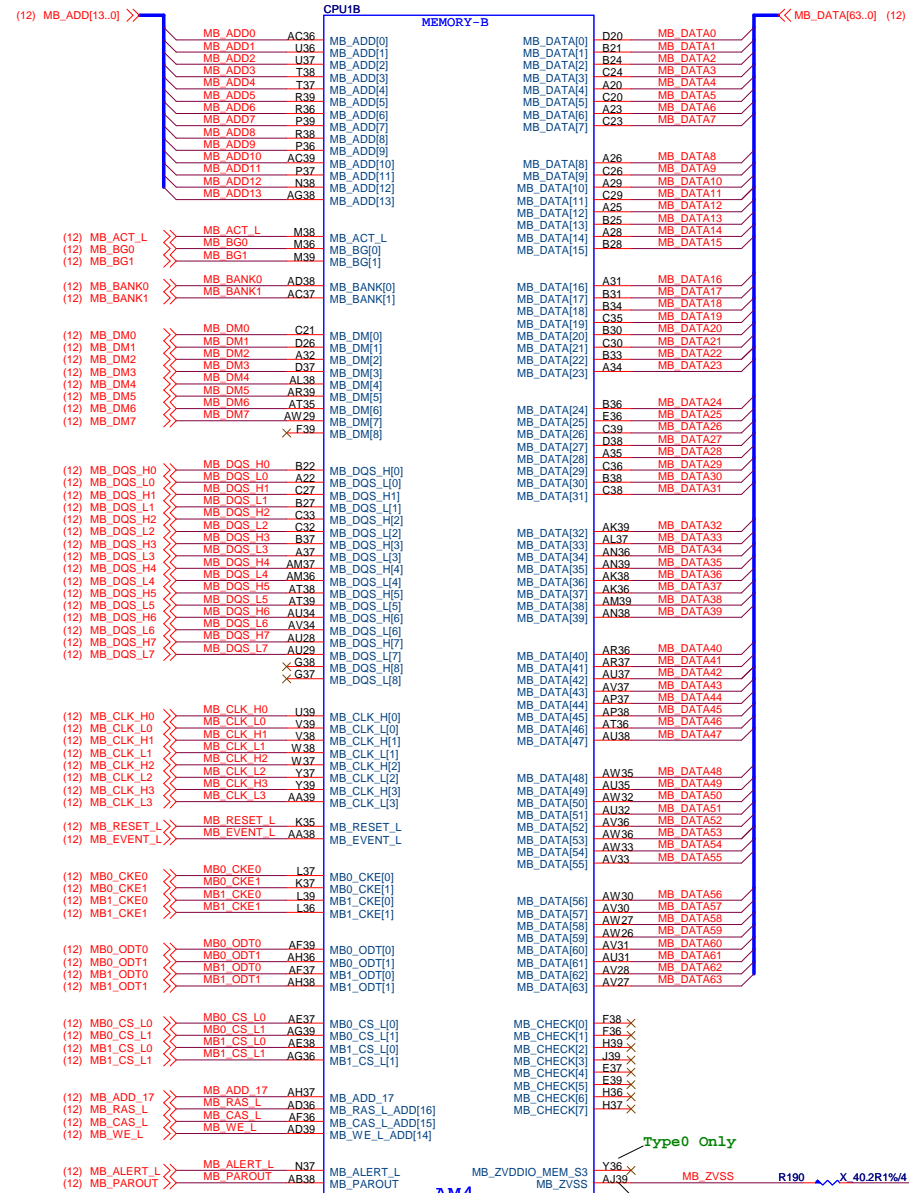
01	Cover Sheet	36	LAN - I211AT	66	MCU - LED Control
02	Block Diagram	37	Audio ALC1220P-VB	67	LED - Power / JPIPE
03	FM4 DDR4 I / F	38	Audio DePop	68	LED - JLED1 / 2 / 3 / 4
04	AM4 PCIE / SATAE	39	USB Power - UP7501	69	LED - Mystic Light - 1
05	AM4 Display / Audio	40	Front USB2.0 Header	70	LED - Mystic Light - 2
06	AM4 SVI / ACPI / GPIO	41	Front USB3.0 Header	71	BOM Option
07	AM4 LPC / SPI / USB / CLK / STRAP	42	Rear USB3.0 + PS2	72	Manual Parts
08-09	AM4 Power / VDDIO_AUDIO Power / GND	43	Rear USB3.0	73	PG MAP
10	RTC / CMOS	44	Rear USB3.1 Type A / redrive	74	GPIO MAP
11-14	DDR4 - POWER / GND	45	Rear USB3.1 Type A / mux	75	Power Sequence
15	Promontory - PCIE / SATA / SATAE	46	DP	76	Power Delivery
16	Promontory - USB / OC	47	HDMI	77	History
17	Promontory - CLK / ACPI / GPIO	48	CPU power UP9505 10+2		
18-19	Promontory - Power / GND	49	CPU power Phase 1-4		
20	PCI_E2 (X16)	50	CPU power Phase 5-10		
21	PCI_E4 (X8)	51	CPU power NB 1-2		
22	PCIE Switch X16 / X8	52	CPU power NB_S5		
23	PCI_E1_E3_E5 (X1)	53	CPU power 1.8_S0 / S5		
24	PCI_E6 (X4)	54	CPU power VDDP - TPS56C215		
25	PCIE Switch X4 / M2_2	55	VRM PWRGD		
26	M.2_1	56	DDR Power - RT8125E		
27	M.2_2	57	DDR Power - VPP25 / VTT		
28	M.2_3 (WIFI+BT)	58	PROM - SY8288RAC / 1.05V		
29	SIO NCT6797D-M	59	PROM - GS7133 / 2.5V		
30	SIO HW Monitor / NCT7718W	60	OV Control - NCT3933		
31	FAN TYPE-J CPUFAN1	61	OV 12VIN - RT9553B		
32	FAN TYPE-J PUMPFAN1	62	ACPI - 3VSB / 5VDIMM		
33	FAN TYPE-K SYSFAN1/2	63	ATX Power - FrpntPanel / EMI		
34	FAN TYPE-K SYSFAN3/4	64	LED - EZDEBUG / AMP		
35	FAN GPIO NCT5605	65	LED - DIMM / PCIE SLOT		





PART 1 OF 9

N12-331A030-L06 ZIF-SOCKET1331



PART 2 OF 9

N12-331A030-L06 ZIF-SOCKET1331



MICRO-STAR INT'L CO.,LTD

MS-7C37

Size	Document Description	Rev
Custom	AM4 DDR4 I/F	3.1
Date: Monday, May 06, 2019/		
Sheet 3 of 75		

TYPE	PCIE	SATA
TYPE 0/1	2	2
TYPE 2/3/4	2 or 4	2 or 0

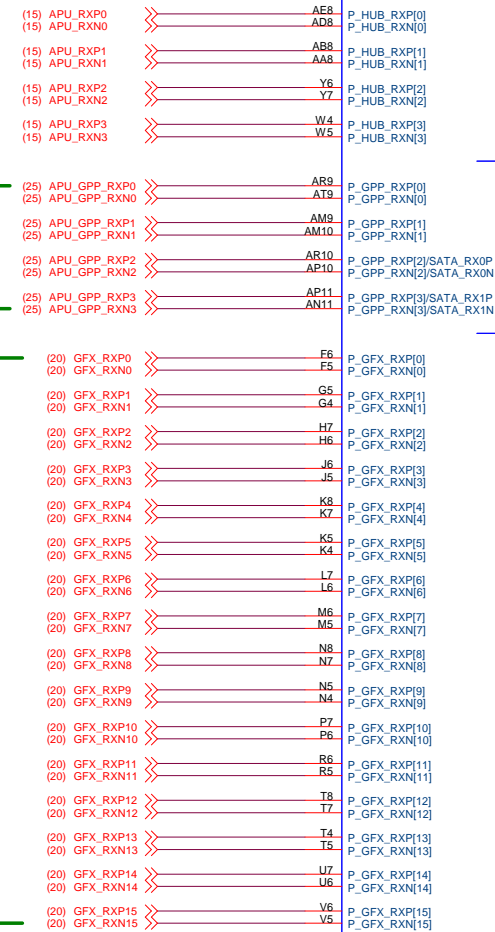
PCI_E1 X16
(For Type-2/4)

Type1 Not Supported GFX 4~15

Type3 Not Support GFX 8~15

M2_1

Type 1: Raven Ridge Only SATA



Within 1500 mils from APU

Within 1000 mils from APU

AM4

PART 3 OR 9

N42-331A030-L06

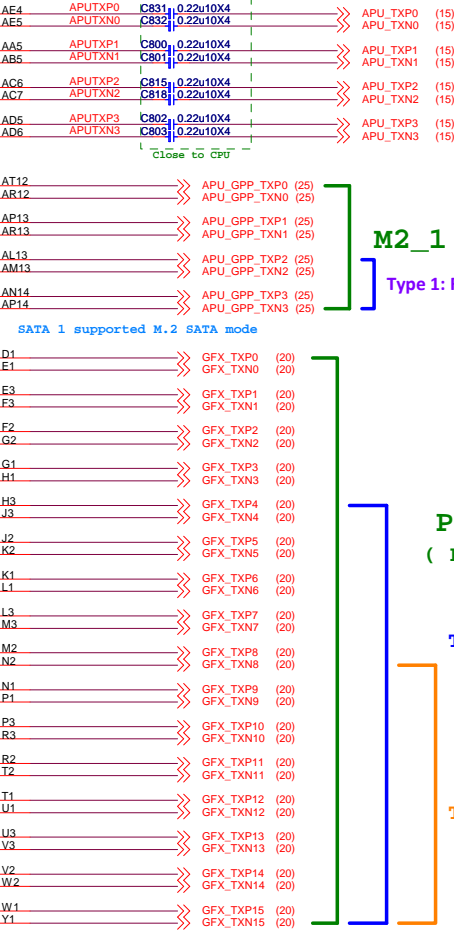
ZIF-SOCKET1331

SATA Express

CPU1C

PCIE

SATA 1 supported M.2 SATA mode



M2_1

Type 1: Raven Ridge Only SATA

PCI_E1 X16
(For Type-2/4)

Type1 Not Supported GFX 4~15

Type3 Not Support GFX 8~15

Within 1500 mils from APU
Within 1500 mils from APU
Within 1000 mils from APU
Within 1000 mils from APU

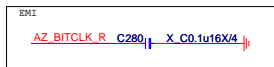
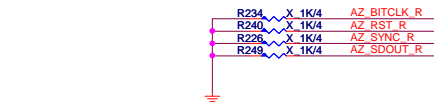
Vinafix.com



MICRO-STAR INT'L CO.,LTD

MS-7C37

Size	Document Description	Rev
Custom	AM4 PCIE / SATAE	3.1
Date: Monday, May 06, 2019	Sheet 4 of 75	



CPU_1P8_S5

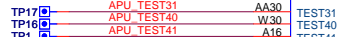
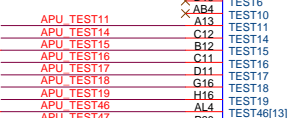
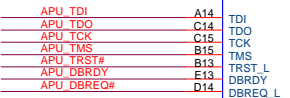
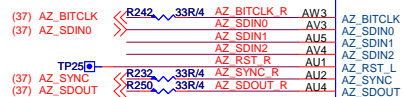


3VSB



For Debug1

For Debug2



CPU1D



AUDIO

DISPLAY-0

DISPLAY-1

TEST

DISPLAY-2

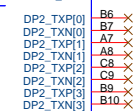
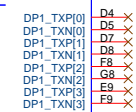
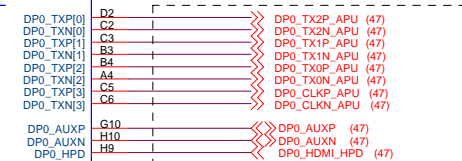
AM4

PART 4 OF 9

N12-331A030-L06

ZIF-SOCKET1331

For HDMI



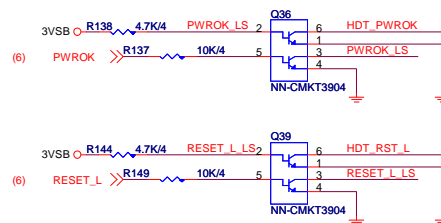
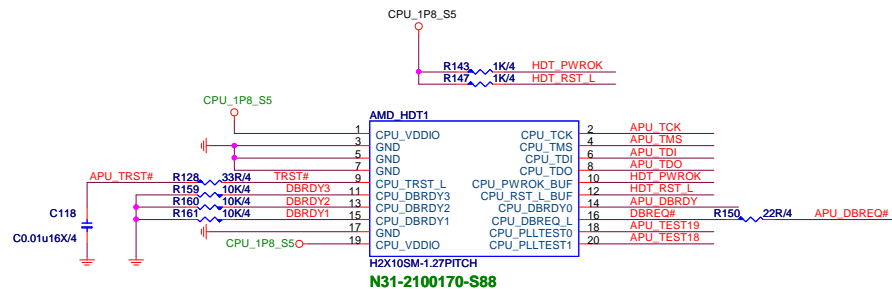
Not supported on TYPE 2/4

Type0 Only

For Debug2

Not support Type2

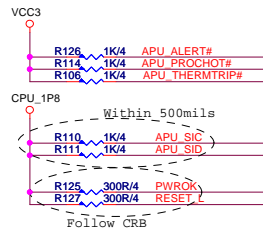
K14 PIN: 有HDMI SPEC的話請Pull-up
ENABLE功能



MICRO-STAR INT'L CO.,LTD

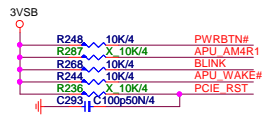
MS-7C37

Size	Document Description	Rev
Custom	AM4 Display / Audio	3.1
Date:	Monday, May 06, 2019	Sheet 5 of 75

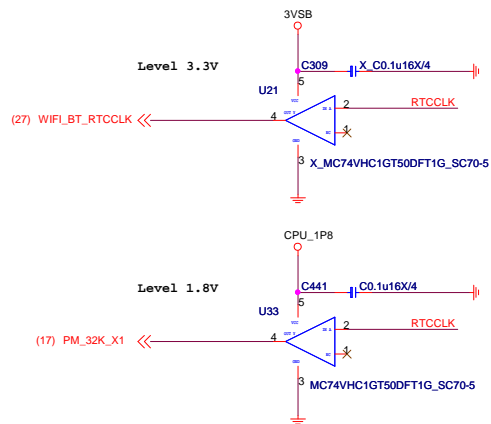
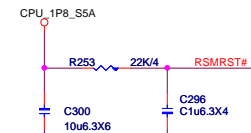
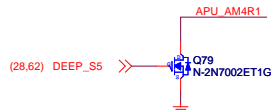


(5) PWROK >>> PWROK
(5) RESET_L >>> RESET_L

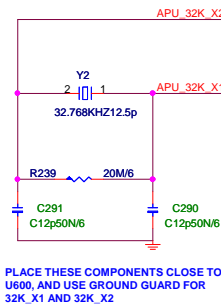
Add for HDT and
close to PIN E16 & B16



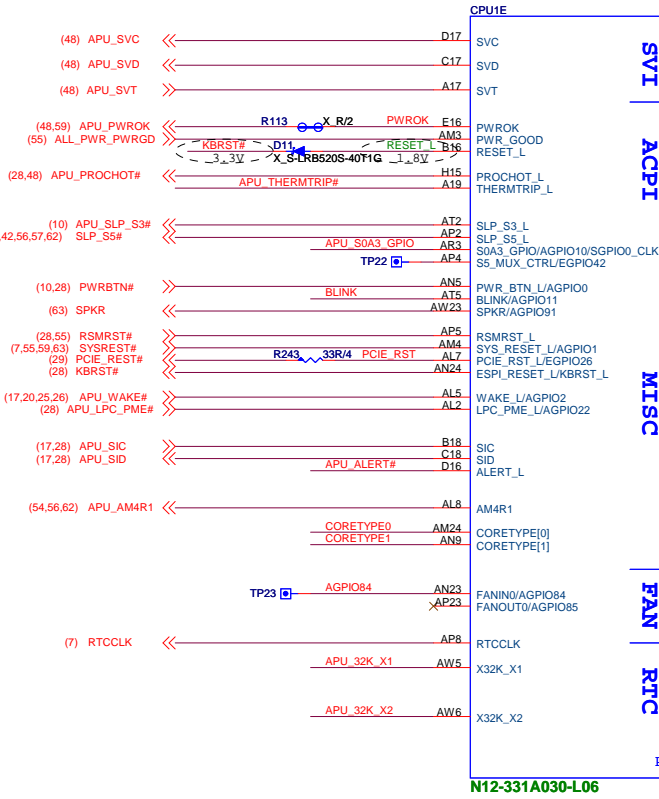
Turn off power when
BIOS into deep mode



Layout:Place x'tal within 1.5 inch of APU



AM4 CPU TYPE Circuit



N12-331A030-L06

$$I_B = (CPU_1P8_S5 - V_{be}) / 5.7k$$

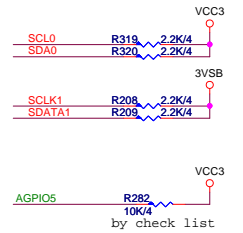
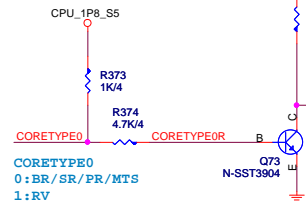
$$(1.8 - 0.95) / 5.7k = 0.149mA$$

$$I_C = (VCC5 - V_{ce}) / 47k$$

$$(5 - 0.2) / 47k = 0.102mA$$

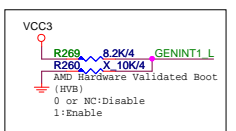
TYPE0_CPU_SEL
0:RV
1:BR/SR/PR/MTS

TYPE0_CPU_SEL (7,54,55)

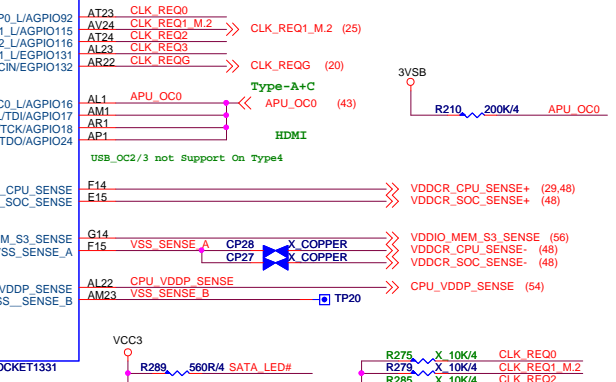


For CNTL M.2 PCIE or SATA

For Select Auto or Manual



GPIO97-100 for Debug LED



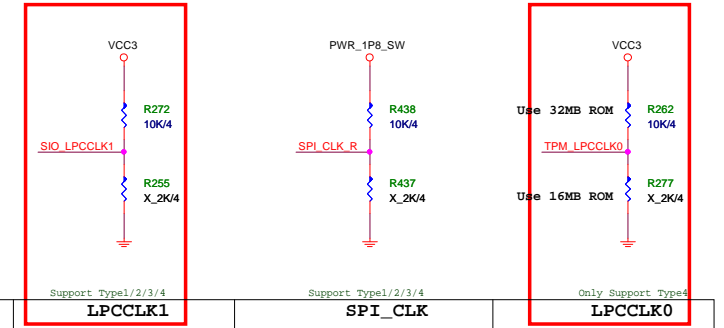
SPEC no Support

CPU	TYPE	CORETYPE 1	CORETYPE 0
BR	0	0	0
NA		0	1
SR	2	1	0
RV/ZP	3	1	1
MTS	4	1	1

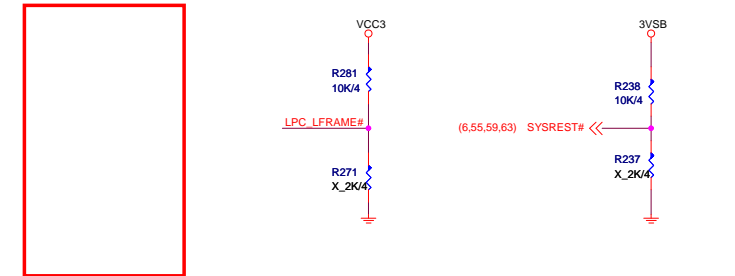


MICRO-STAR INT'L CO.,LTD			
MS-7C37			
Size	Document Description	Rev	
Custom	AM4 SVI/ACPI/GPIO	3.1	
Date:	Monday, May 06, 2019	Sheet	6 of 75

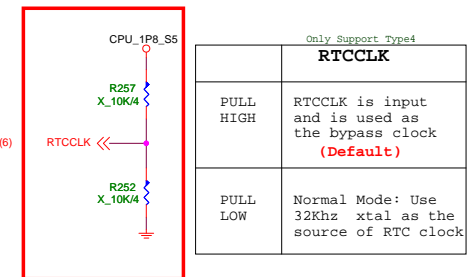
Strapping Options



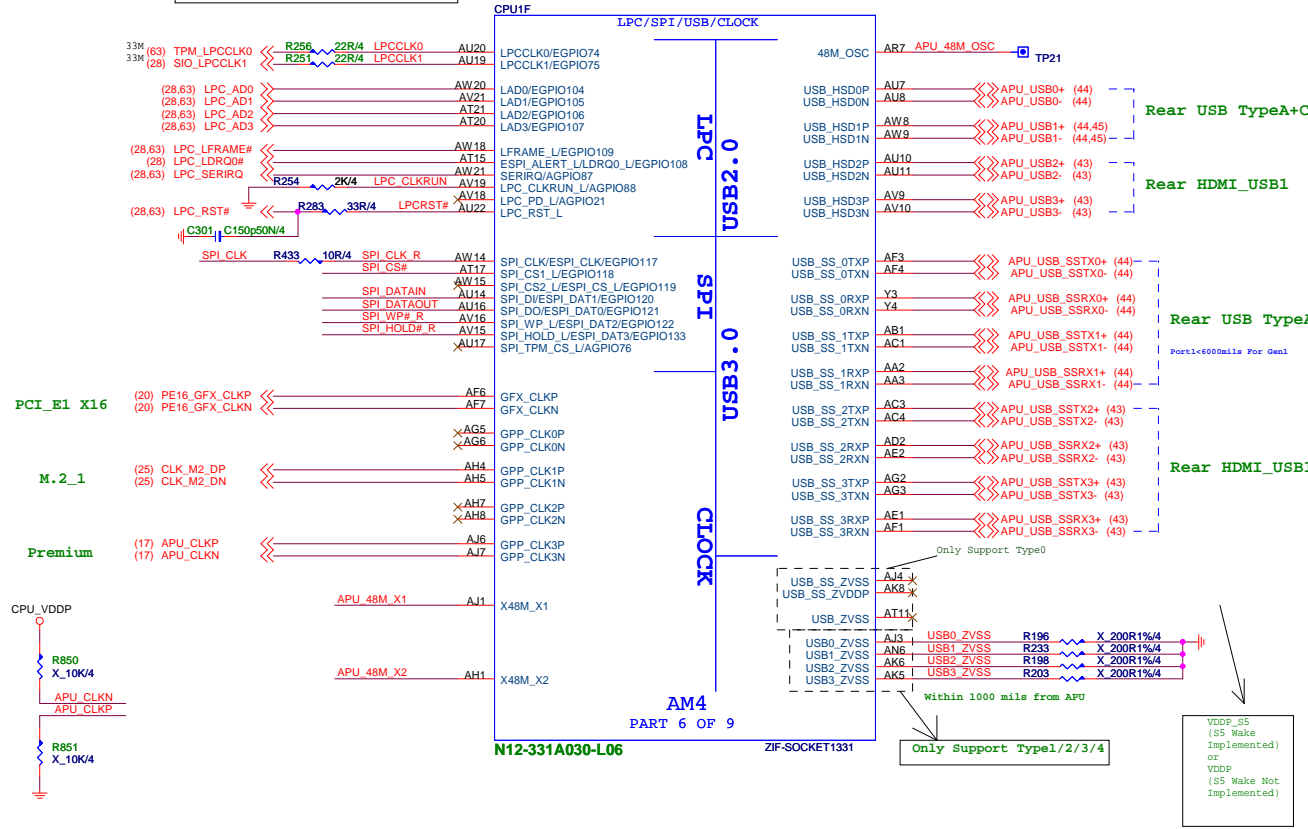
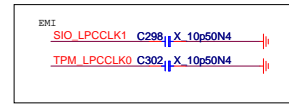
	LPCCLK1	SPI_CLK	LPCCLK0
PULL HIGH	Configured for Internal clock generator (Default)	Use 48Mhz crystal clock and generate both internal and external clocks (Default)	PSP should modify SPI page register bits [25:24] to remap physical ROM to upper image (Default)
PULL LOW	Configured for External clock generator ?????	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	PSP should not modify SPI page register bits [25:24]



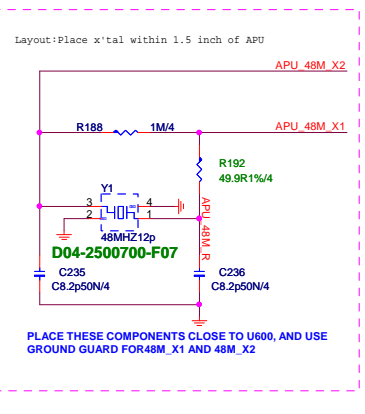
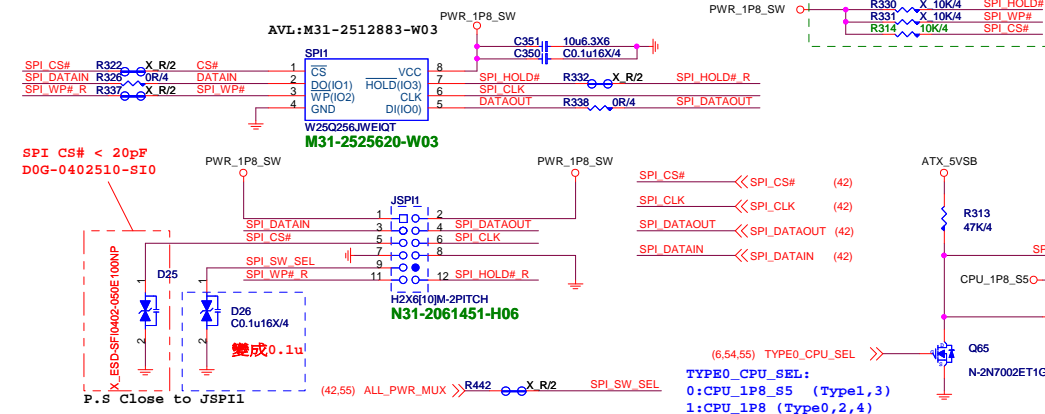
	AGPIO3	LFRAME	SYSREST#
PULL HIGH	Enhanced Reset logic (Default)	SPI ROM (Default)	Normal reset mode (Default)
PULL LOW	Traditional Reset logic	LPC ROM	short reset mode

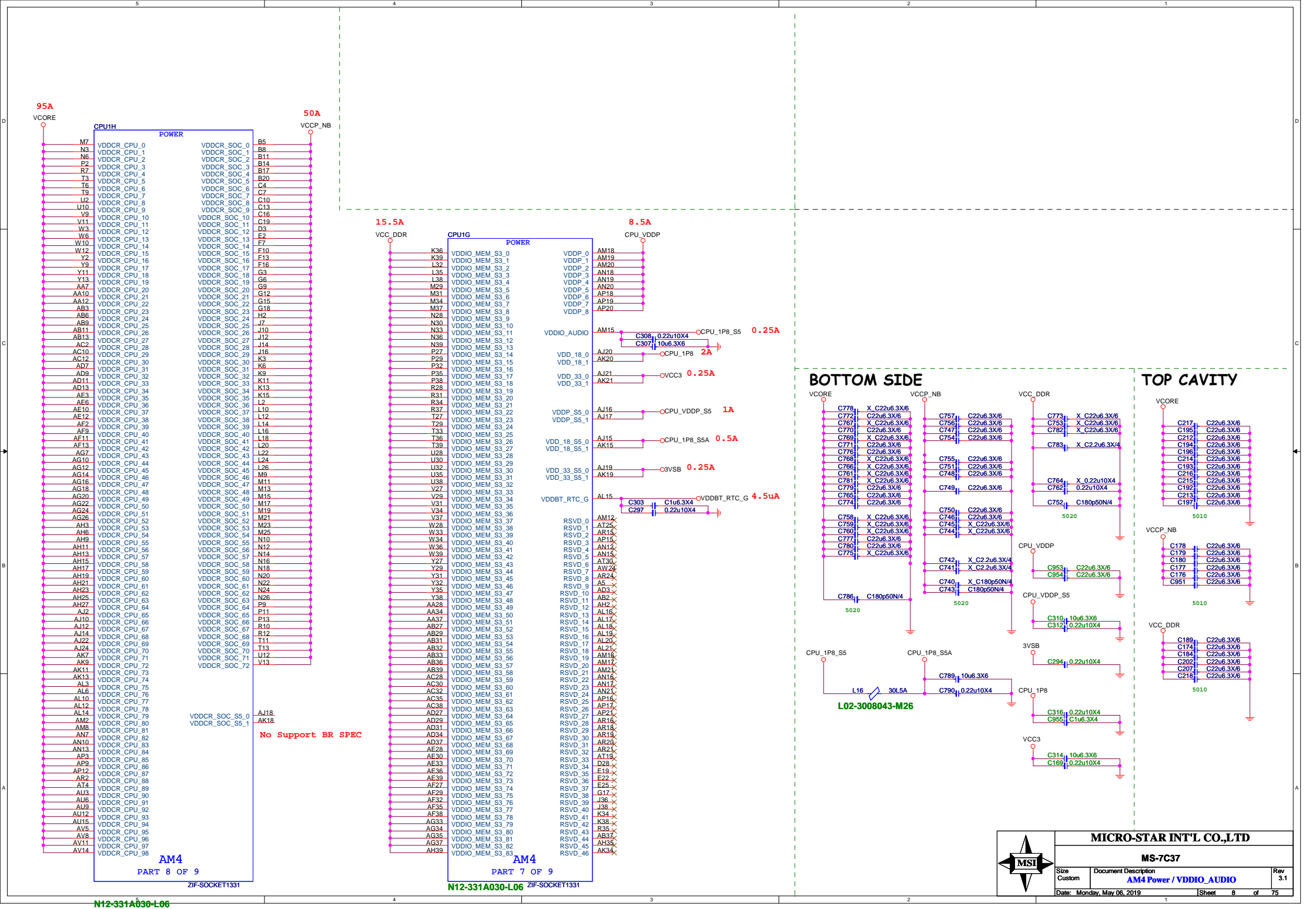


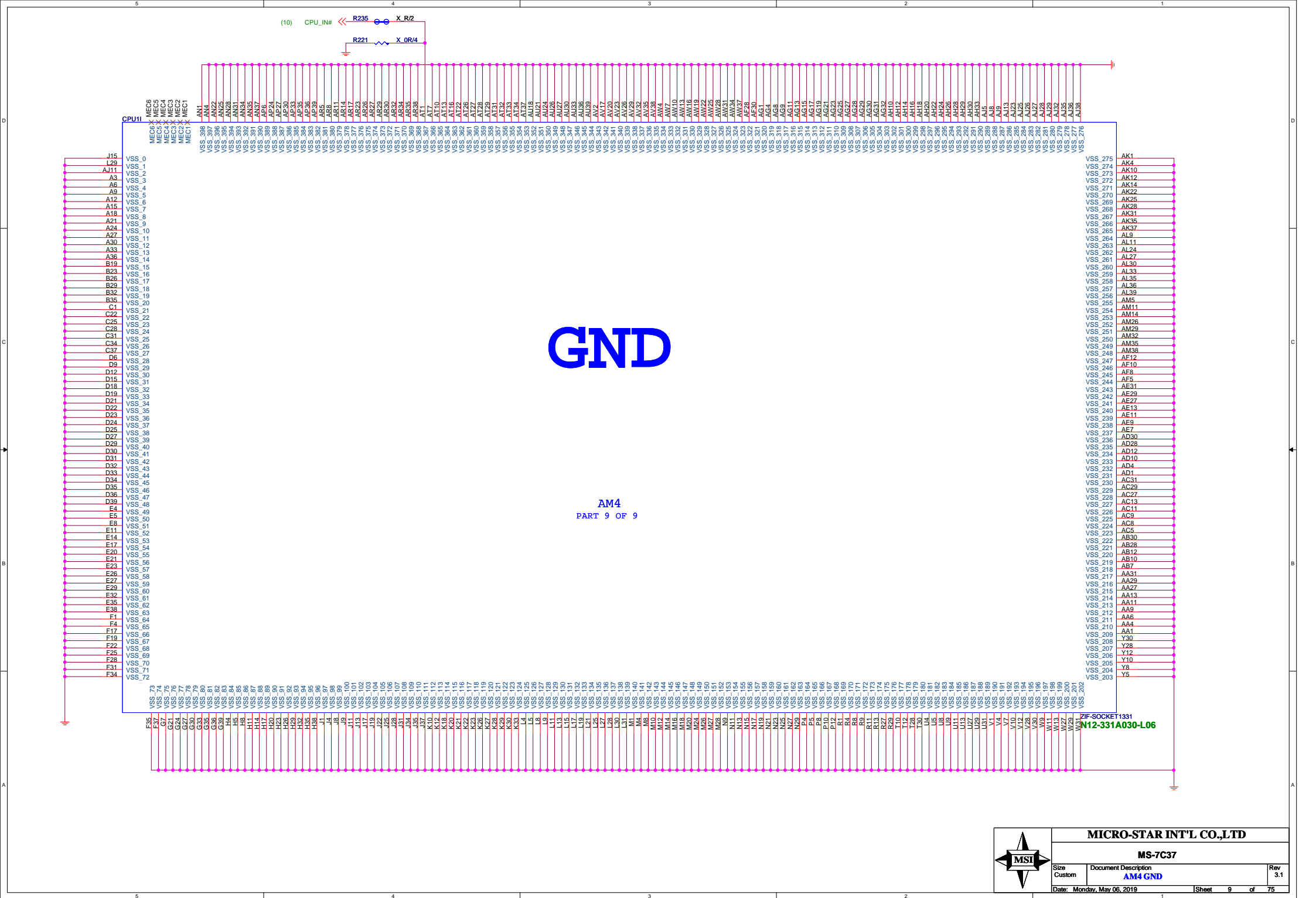
MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size Custom	Document Description	Rev 3.1
AM4/LPC/SPI/USB/CLK/STRAP		
Date: Monday, May 06, 2019	Sheet 7	of 75



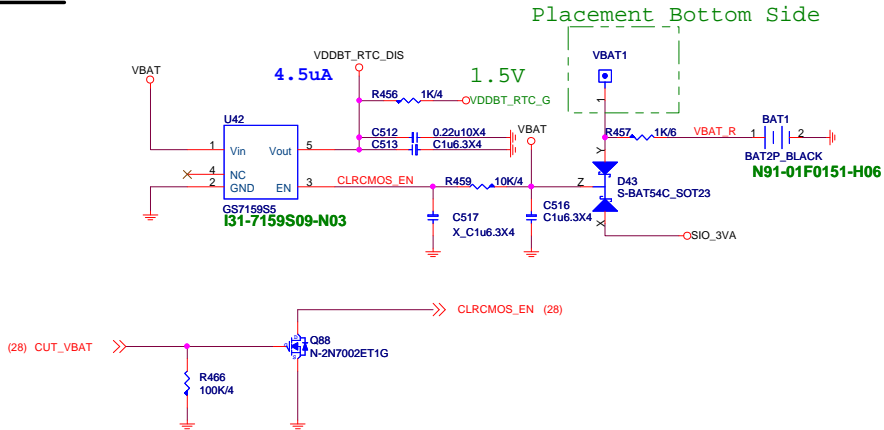
SPI ROM(1.8V)



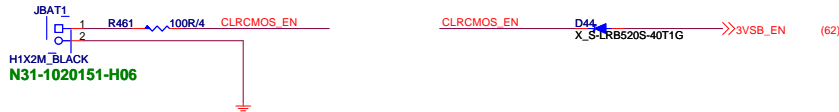




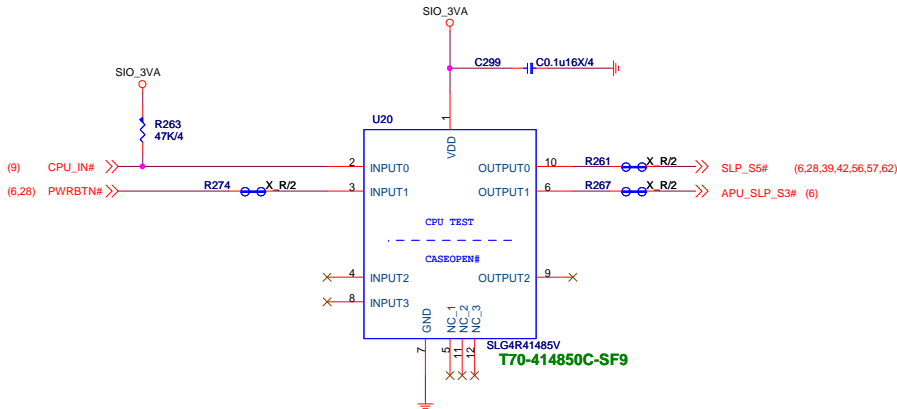
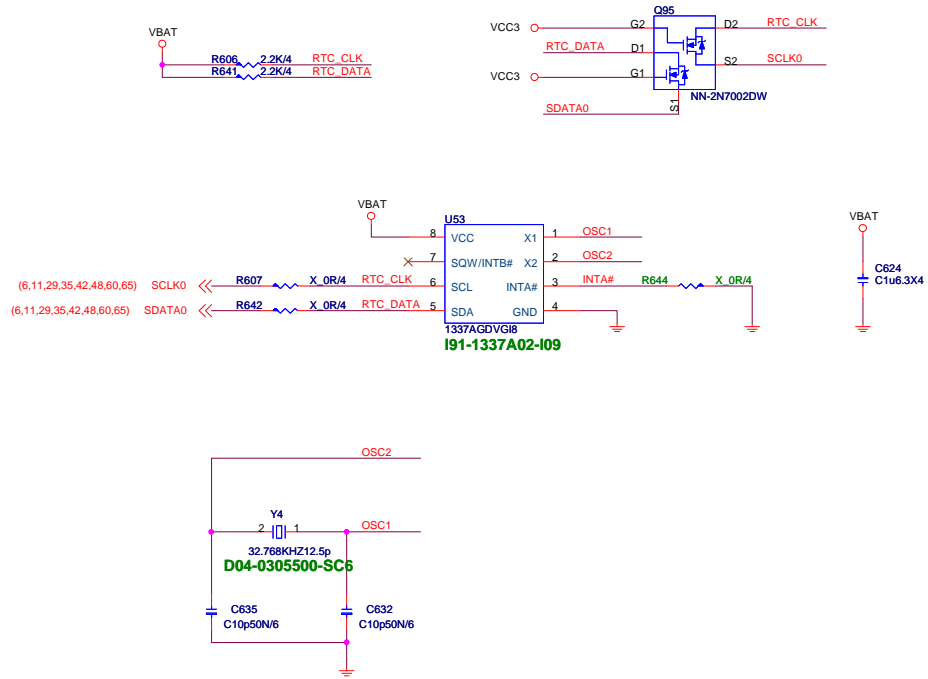
RTC & Clear CMOS Circuit



Clear CMOS button



RTC Backup



A1 A2 B1 B2

DIMMA1A

QDS17P MA DATA63
QDS17N MA DATA62
QDS16P MA DATA61
QDS16N MA DATA60
QDS15P MA DATA59
QDS15N MA DATA58
QDS14P MA DATA57
QDS14N MA DATA56
QDS13P MA DATA55
QDS13N MA DATA54
QDS12P MA DATA53
QDS12N MA DATA52
QDS11P MA DATA51
QDS11N MA DATA50
QDS10P MA DATA49
QDS10N MA DATA48
QDS9P MA DATA47
QDS9N MA DATA46
QDS8P MA DATA45
QDS8N MA DATA44
QDS7P MA DATA43
QDS7N MA DATA42
QDS6P MA DATA41
QDS6N MA DATA40
QDS5P MA DATA39
QDS5N MA DATA38
QDS4P MA DATA37
QDS4N MA DATA36
QDS3P MA DATA35
QDS3N MA DATA34
QDS2P MA DATA33
QDS2N MA DATA32
QDS1P MA DATA31
QDS1N MA DATA30
QDS0P MA DATA29
QDS0N MA DATA28
QDS0P MA DATA27
QDS0N MA DATA26
QDS0P MA DATA25
QDS0N MA DATA24
QDS0P MA DATA23
QDS0N MA DATA22
QDS0P MA DATA21
QDS0N MA DATA20
QDS0P MA DATA19
QDS0N MA DATA18
QDS0P MA DATA17
QDS0N MA DATA16
QDS0P MA DATA15
QDS0N MA DATA14
QDS0P MA DATA13
QDS0N MA DATA12
QDS0P MA DATA11
QDS0N MA DATA10
QDS0P MA DATA9
QDS0N MA DATA8
QDS0P MA DATA7
QDS0N MA DATA6
QDS0P MA DATA5
QDS0N MA DATA4
QDS0P MA DATA3
QDS0N MA DATA2
QDS0P MA DATA1
QDS0N MA DATA0

C2
S3_N_C1
S2_N_C0

MA0_CS_L1
MA0_CS_L0
MA0_CKE1
MA0_CKE0
MA0_ODT1
MA0_ODT0

CB-7
CB-6
CB-5
CB-4
CB-3
CB-2
CB-1
CB-0

MA_RESET_L
MA_EVENT_L
MA_ALERT_L
MA_ACT_L
MA_PAROUT

SAVE_N_NC
RFU-0
RFU-1
RFU-2

DDRIV-288P_BLACK
N13-2880551-L06

DQ-63 MA DATA63
DQ-62 MA DATA62
DQ-61 MA DATA61
DQ-60 MA DATA60
DQ-59 MA DATA59
DQ-58 MA DATA58
DQ-57 MA DATA57
DQ-56 MA DATA56
DQ-55 MA DATA55
DQ-54 MA DATA54
DQ-53 MA DATA53
DQ-52 MA DATA52
DQ-51 MA DATA51
DQ-50 MA DATA50
DQ-49 MA DATA49
DQ-48 MA DATA48
DQ-47 MA DATA47
DQ-46 MA DATA46
DQ-45 MA DATA45
DQ-44 MA DATA44
DQ-43 MA DATA43
DQ-42 MA DATA42
DQ-41 MA DATA41
DQ-40 MA DATA40
DQ-39 MA DATA39
DQ-38 MA DATA38
DQ-37 MA DATA37
DQ-36 MA DATA36
DQ-35 MA DATA35
DQ-34 MA DATA34
DQ-33 MA DATA33
DQ-32 MA DATA32
DQ-31 MA DATA31
DQ-30 MA DATA30
DQ-29 MA DATA29
DQ-28 MA DATA28
DQ-27 MA DATA27
DQ-26 MA DATA26
DQ-25 MA DATA25
DQ-24 MA DATA24
DQ-23 MA DATA23
DQ-22 MA DATA22
DQ-21 MA DATA21
DQ-20 MA DATA20
DQ-19 MA DATA19
DQ-18 MA DATA18
DQ-17 MA DATA17
DQ-16 MA DATA16
DQ-15 MA DATA15
DQ-14 MA DATA14
DQ-13 MA DATA13
DQ-12 MA DATA12
DQ-11 MA DATA11
DQ-10 MA DATA10
DQ-9 MA DATA9
DQ-8 MA DATA8
DQ-7 MA DATA7
DQ-6 MA DATA6
DQ-5 MA DATA5
DQ-4 MA DATA4
DQ-3 MA DATA3
DQ-2 MA DATA2
DQ-1 MA DATA1
DQ-0 MA DATA0

BG-1 MA BG1
BG-0 MA BG0

BA-1 MA BANK1
BA-0 MA BANK0

A17 MA ADD 17
A16_RAS_N MA RAS_L
A15_CAS_N MA CAS_L
A14_WE_N MA WE_L

A13 MA ADD12
A12 MA ADD11
A11 MA ADD10
A10 MA ADD9
A9 MA ADD8
A8 MA ADD7
A7 MA ADD6
A6 MA ADD5
A5 MA ADD4
A4 MA ADD3
A3 MA ADD2
A2 MA ADD1
A1 MA ADD0

SCL SMB_CLK_DIMM
SDA SMB_DATA_DIMM

SA-2
SA-1
SA-0

DIMM1 (CHANNEL-A) -A0
ADDRESS = 0:0 [SA1:SA0]

<< MA_DATA[63..0] (3)

56-63

48-55

40-47

32-39

24-31

16-23

8-15

0-7

teknisi indonesia

SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMB0	A2
DIMMB1	A6

VCC_DDR
R186 1K/4

DIMMA2A

QDS17P MA DATA63
QDS17N MA DATA62
QDS16P MA DATA61
QDS16N MA DATA60
QDS15P MA DATA59
QDS15N MA DATA58
QDS14P MA DATA57
QDS14N MA DATA56
QDS13P MA DATA55
QDS13N MA DATA54
QDS12P MA DATA53
QDS12N MA DATA52
QDS11P MA DATA51
QDS11N MA DATA50
QDS10P MA DATA49
QDS10N MA DATA48
QDS9P MA DATA47
QDS9N MA DATA46
QDS8P MA DATA45
QDS8N MA DATA44
QDS7P MA DATA43
QDS7N MA DATA42
QDS6P MA DATA41
QDS6N MA DATA40
QDS5P MA DATA39
QDS5N MA DATA38
QDS4P MA DATA37
QDS4N MA DATA36
QDS3P MA DATA35
QDS3N MA DATA34
QDS2P MA DATA33
QDS2N MA DATA32
QDS1P MA DATA31
QDS1N MA DATA30
QDS0P MA DATA29
QDS0N MA DATA28
QDS0P MA DATA27
QDS0N MA DATA26
QDS0P MA DATA25
QDS0N MA DATA24
QDS0P MA DATA23
QDS0N MA DATA22
QDS0P MA DATA21
QDS0N MA DATA20
QDS0P MA DATA19
QDS0N MA DATA18
QDS0P MA DATA17
QDS0N MA DATA16
QDS0P MA DATA15
QDS0N MA DATA14
QDS0P MA DATA13
QDS0N MA DATA12
QDS0P MA DATA11
QDS0N MA DATA10
QDS0P MA DATA9
QDS0N MA DATA8
QDS0P MA DATA7
QDS0N MA DATA6
QDS0P MA DATA5
QDS0N MA DATA4
QDS0P MA DATA3
QDS0N MA DATA2
QDS0P MA DATA1
QDS0N MA DATA0

C2
S3_N_C1
S2_N_C0

MA1_CS_L1
MA1_CS_L0
MA1_CKE1
MA1_CKE0
MA1_ODT1
MA1_ODT0

CB-7
CB-6
CB-5
CB-4
CB-3
CB-2
CB-1
CB-0

MA_RESET_L
MA_EVENT_L
MA_ALERT_L
MA_ACT_L
MA_PAROUT

SAVE_N_NC
RFU-0
RFU-1
RFU-2

DDRIV-288P_BLACK
N13-2880551-L06

DQ-63 MA DATA63
DQ-62 MA DATA62
DQ-61 MA DATA61
DQ-60 MA DATA60
DQ-59 MA DATA59
DQ-58 MA DATA58
DQ-57 MA DATA57
DQ-56 MA DATA56
DQ-55 MA DATA55
DQ-54 MA DATA54
DQ-53 MA DATA53
DQ-52 MA DATA52
DQ-51 MA DATA51
DQ-50 MA DATA50
DQ-49 MA DATA49
DQ-48 MA DATA48
DQ-47 MA DATA47
DQ-46 MA DATA46
DQ-45 MA DATA45
DQ-44 MA DATA44
DQ-43 MA DATA43
DQ-42 MA DATA42
DQ-41 MA DATA41
DQ-40 MA DATA40
DQ-39 MA DATA39
DQ-38 MA DATA38
DQ-37 MA DATA37
DQ-36 MA DATA36
DQ-35 MA DATA35
DQ-34 MA DATA34
DQ-33 MA DATA33
DQ-32 MA DATA32
DQ-31 MA DATA31
DQ-30 MA DATA30
DQ-29 MA DATA29
DQ-28 MA DATA28
DQ-27 MA DATA27
DQ-26 MA DATA26
DQ-25 MA DATA25
DQ-24 MA DATA24
DQ-23 MA DATA23
DQ-22 MA DATA22
DQ-21 MA DATA21
DQ-20 MA DATA20
DQ-19 MA DATA19
DQ-18 MA DATA18
DQ-17 MA DATA17
DQ-16 MA DATA16
DQ-15 MA DATA15
DQ-14 MA DATA14
DQ-13 MA DATA13
DQ-12 MA DATA12
DQ-11 MA DATA11
DQ-10 MA DATA10
DQ-9 MA DATA9
DQ-8 MA DATA8
DQ-7 MA DATA7
DQ-6 MA DATA6
DQ-5 MA DATA5
DQ-4 MA DATA4
DQ-3 MA DATA3
DQ-2 MA DATA2
DQ-1 MA DATA1
DQ-0 MA DATA0

BG-1 MA BG1
BG-0 MA BG0

BA-1 MA BANK1
BA-0 MA BANK0

A17 MA ADD 17
A16_RAS_N MA RAS_L
A15_CAS_N MA CAS_L
A14_WE_N MA WE_L

A13 MA ADD12
A12 MA ADD11
A11 MA ADD10
A10 MA ADD9
A9 MA ADD8
A8 MA ADD7
A7 MA ADD6
A6 MA ADD5
A5 MA ADD4
A4 MA ADD3
A3 MA ADD2
A2 MA ADD1
A1 MA ADD0

SCL SMB_CLK_DIMM
SDA SMB_DATA_DIMM

SA-2
SA-1
SA-0

DIMM2 (CHANNEL-A) -A4
ADDRESS = 1:0 [SA1:SA0]

<< MA_DATA[63..0] (3)

56-63

48-55

40-47

32-39

24-31

16-23

8-15

0-7

VCC3_SPD_A2A1
R303 1K/4

(6,10,29,35,42,48,60,65) SCLK0 SCLK0 R333 X R/2 SMB_CLK_DIMM (12)
(6,10,29,35,42,48,60,65) SDATA0 SDATA0 R328 X R/2 SMB_DATA_DIMM (12)

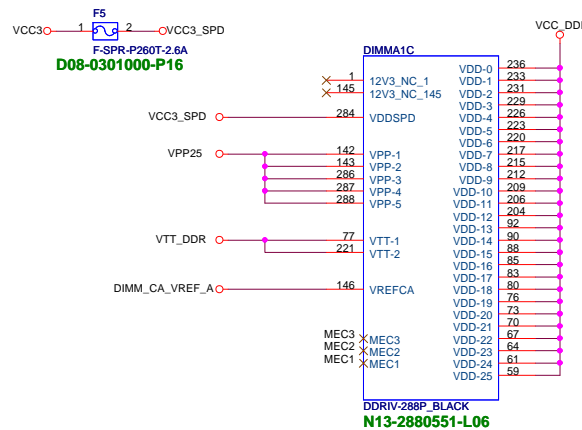


MICRO-STAR INT'L CO.,LTD

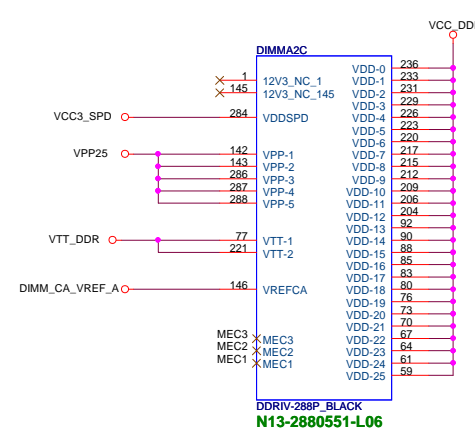
MS-7C37

Size	Document Description	Rev
Custom	DDR4 - DIMM CH-A	3.1
Date: Monday, May 06, 2019% Sheet 11 of 75		

av1:D08-0301100-B07

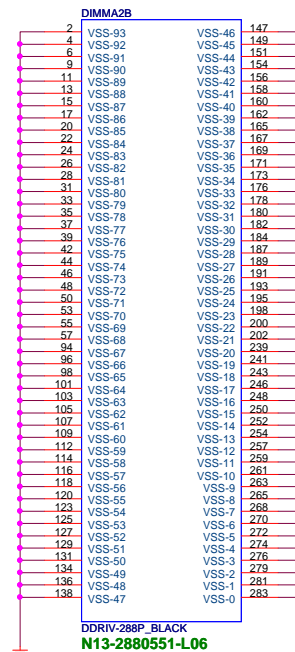
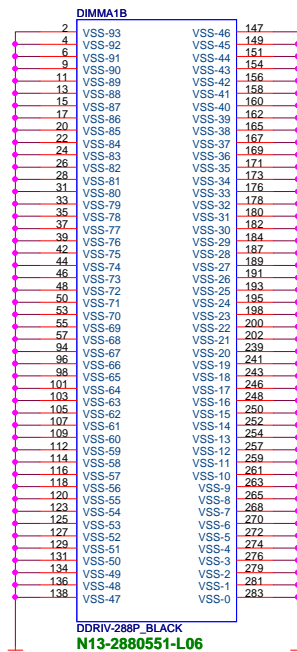
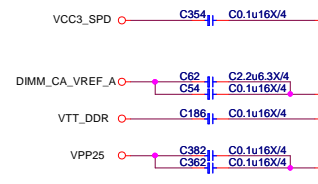
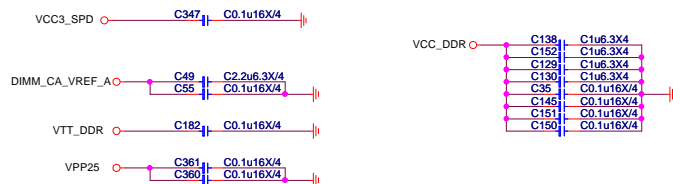
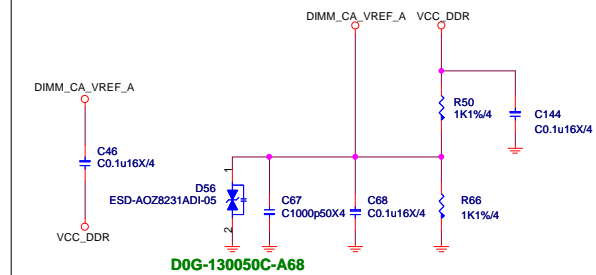


DIMM SLOT PN BY SPEC



DDR VREF

(place resistors close to DIMMs)



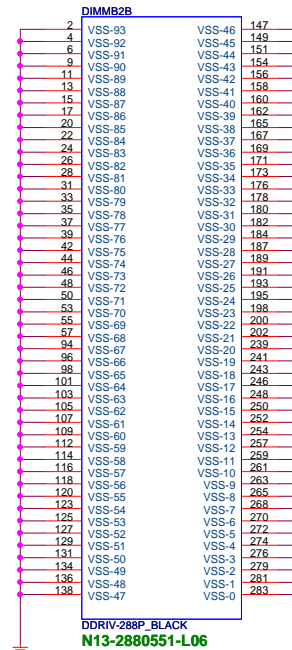
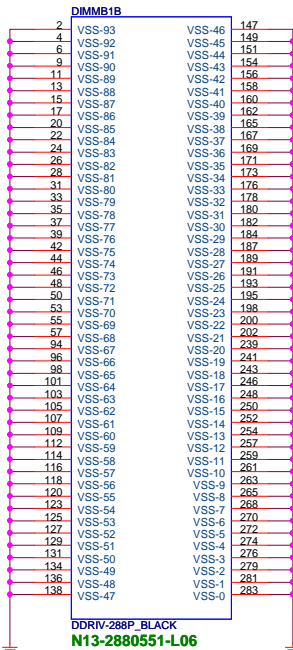
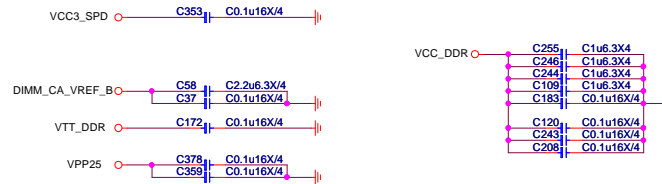
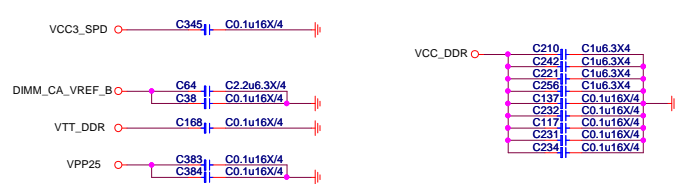
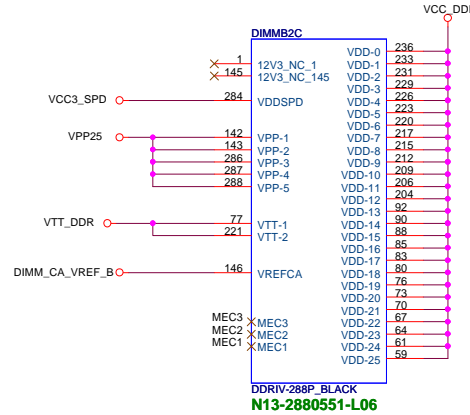
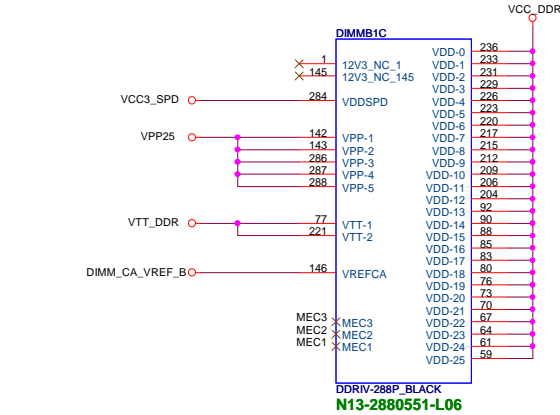
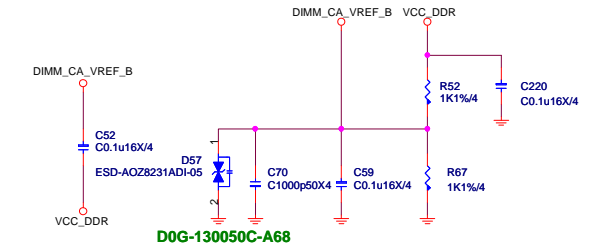
MICRO-STAR INT'L CO.,LTD

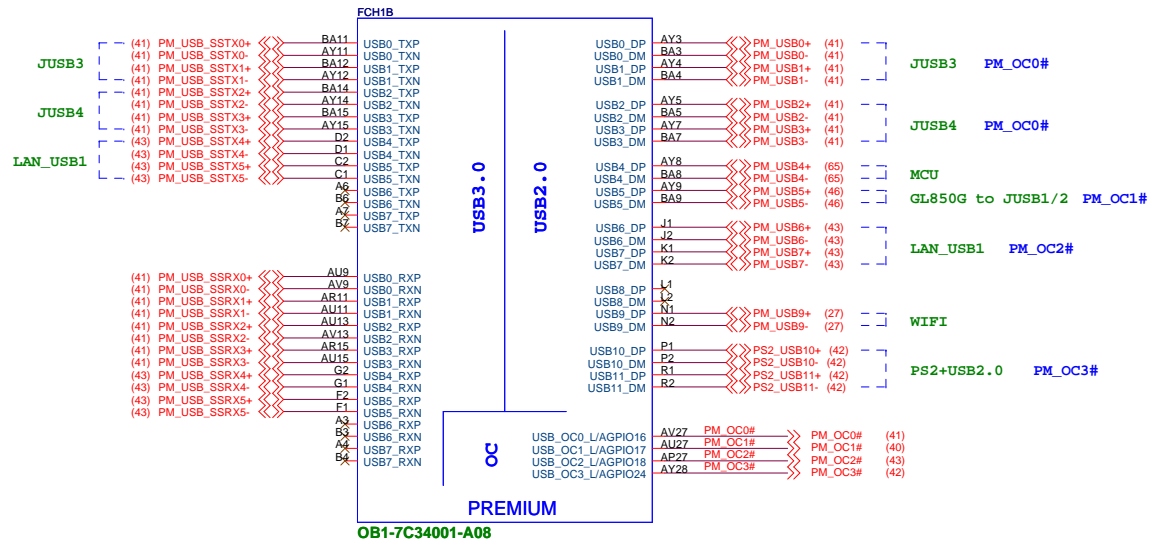
MS-7C37

Size	Document Description	Rev
Custom	DDR4 - POWER/GND-1	3.1
Date:	Monday, May 06, 2019	Sheet 13 of 75

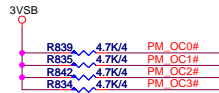
DDR VREF

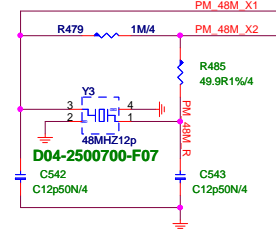
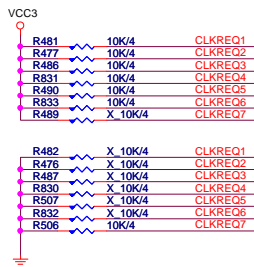
(place resistors close to DIMMs)



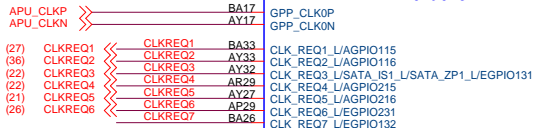


Ports	Host Controller	OC Pins Mapped
USB 3.2 Port 0 - 3 and USB 2.0 Port 0 - 5	Host Controller 0 (HC0)	USB_OC0_L/AGPIO16 USB_OC1_L/AGPIO17
USB 3.2 Port 4 - 7 and USB 2.0 Port 6 - 11	Host Controller 1 (HC1)	USB_OC2_L/AGPIO18 USB_OC3_L/AGPIO24

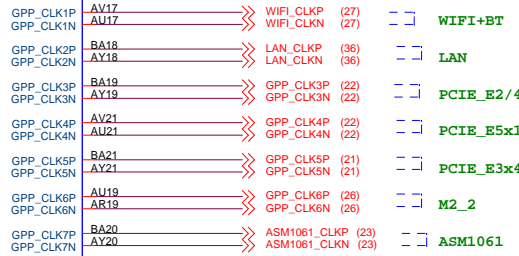




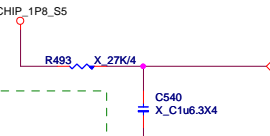
WIFI+BT
LAN
PCIE_E2/4x1
PCIE_E5x1
M.2_2
ASM1061



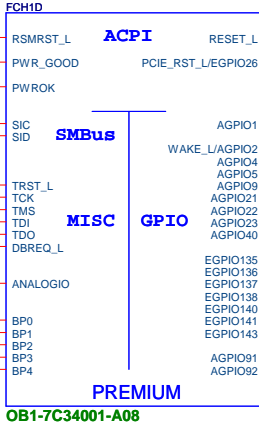
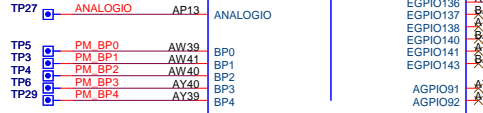
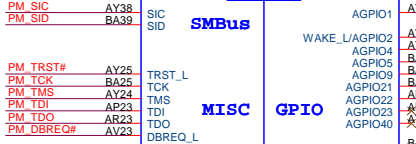
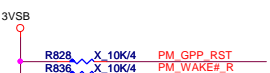
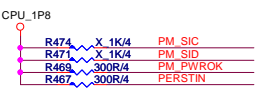
CLOCKS



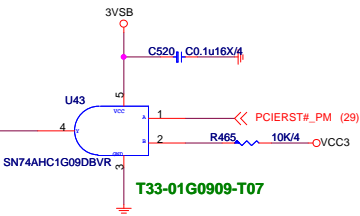
OB1-7C34001-A08



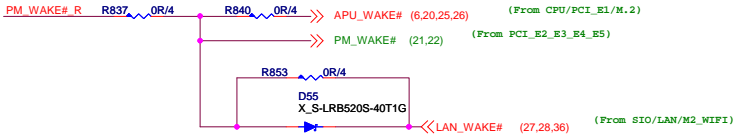
Deplete C549 For PCH FAN ME Interfere



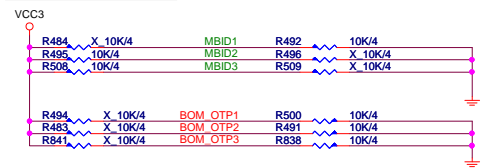
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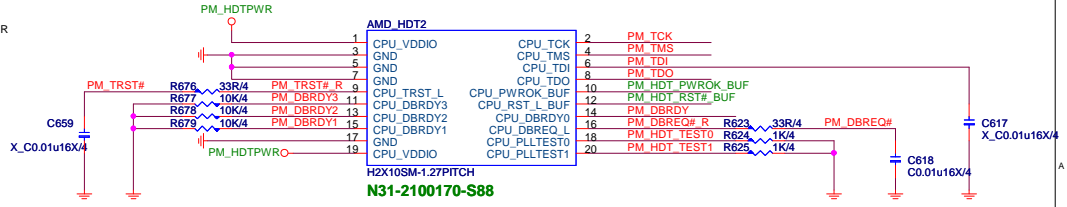
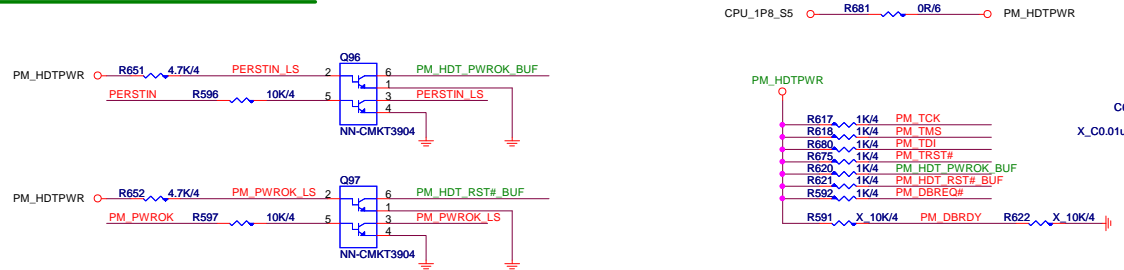
T33-01G0909-T07



BOM OPTION



PREMIUM CHIPSET_HDT



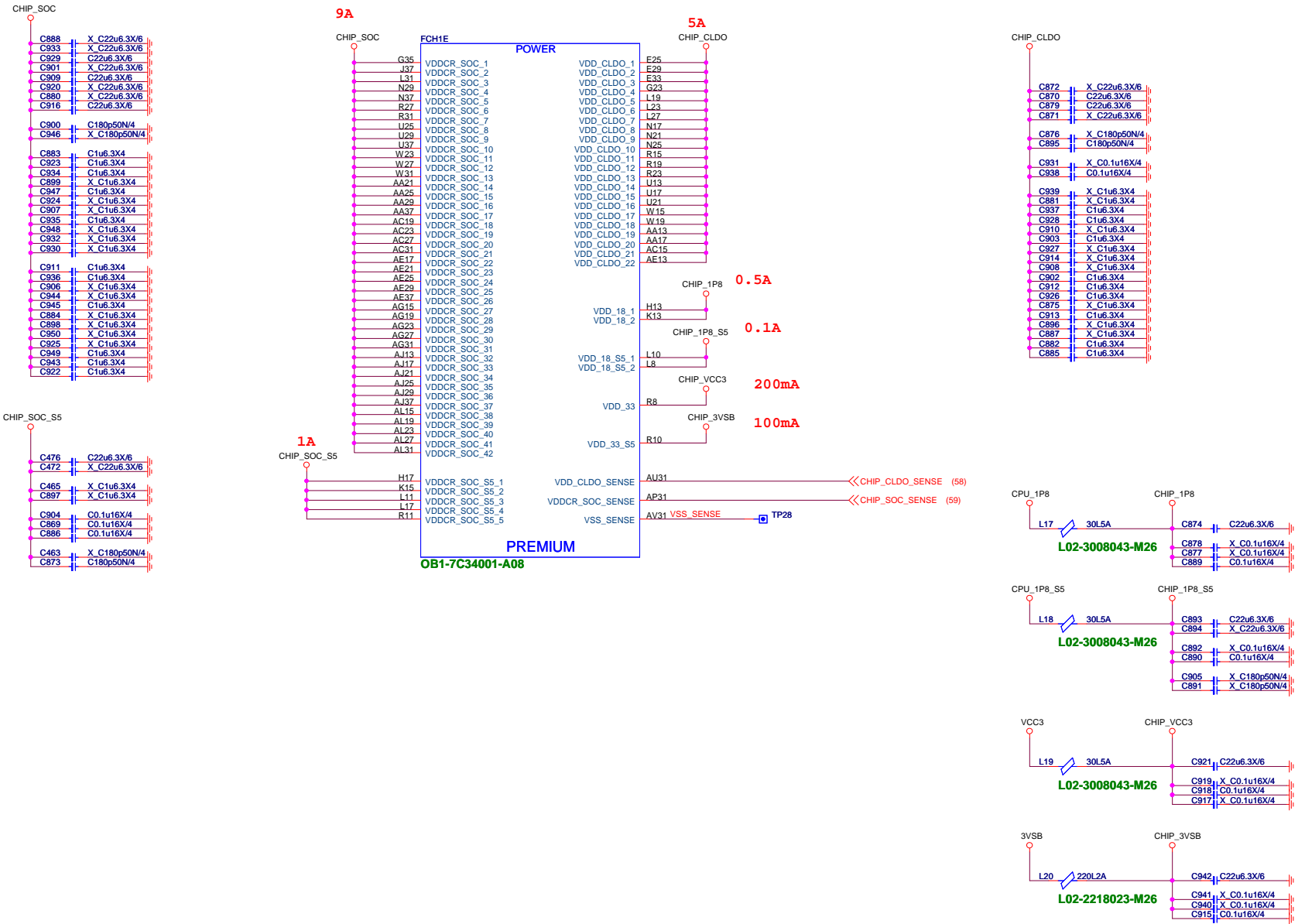
MSI

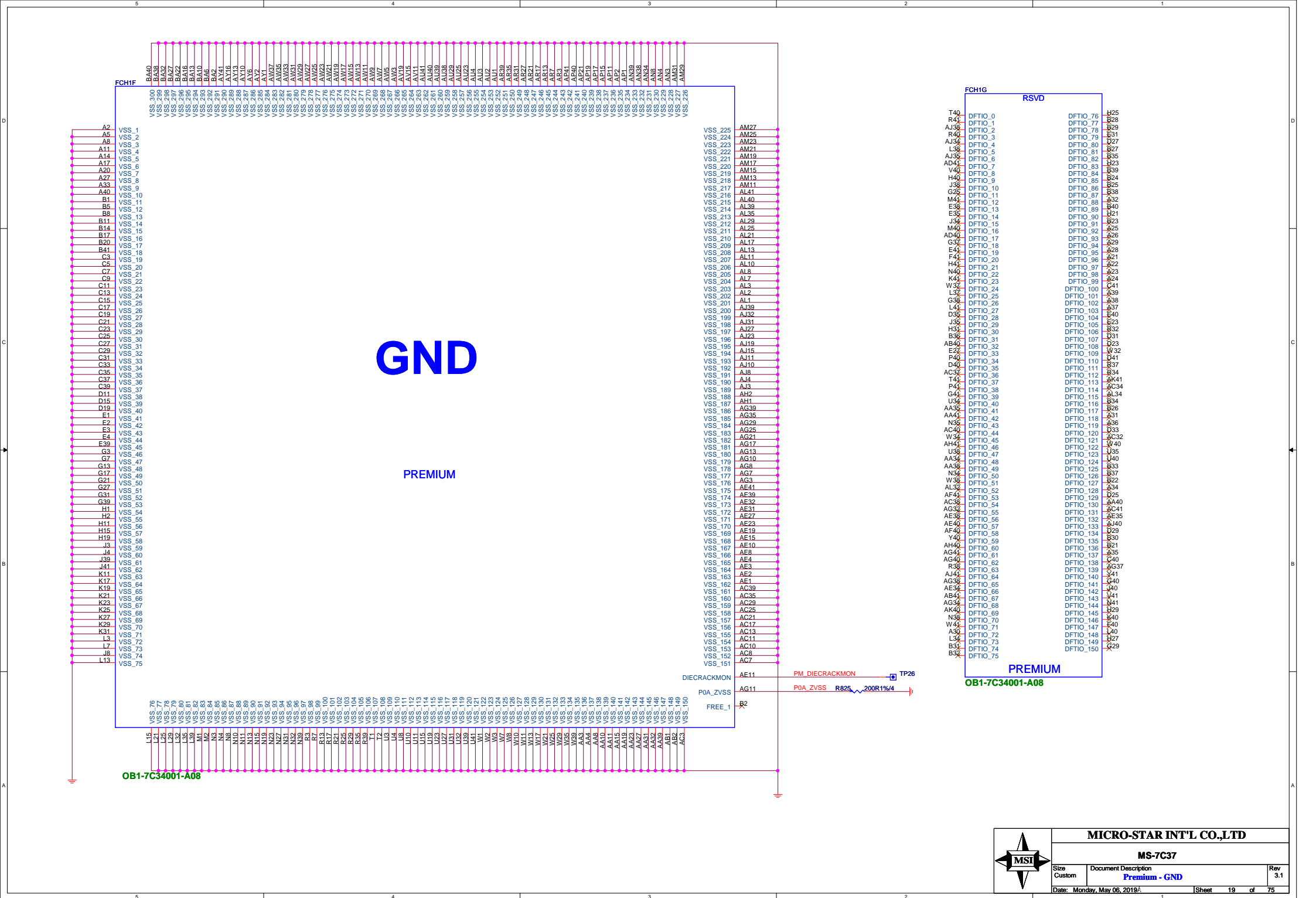
MICRO-STAR INT'L CO.,LTD

MS-7C37

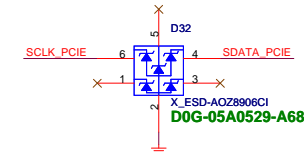
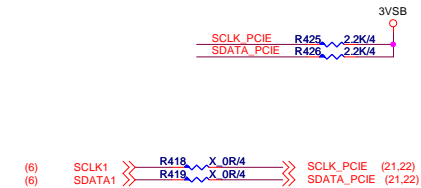
Size Custom Document Description Premium - CLK/ACPI/GPIO Rev 3.1

Date: Monday, May 06, 2019 Sheet 17 of 75





PCI_E1



VCORE

C143

0.1u25X4

VCORE

C170 C171 C268 C181 C275 C272 C173 C190 C267 C260

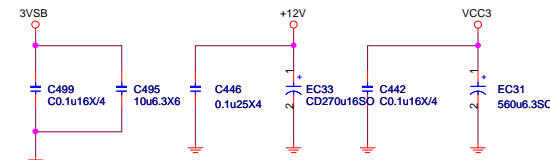
0.1u25X4

VCORE

C259 C262 C263 C245 C269 C264 C270 C257 C258 C273

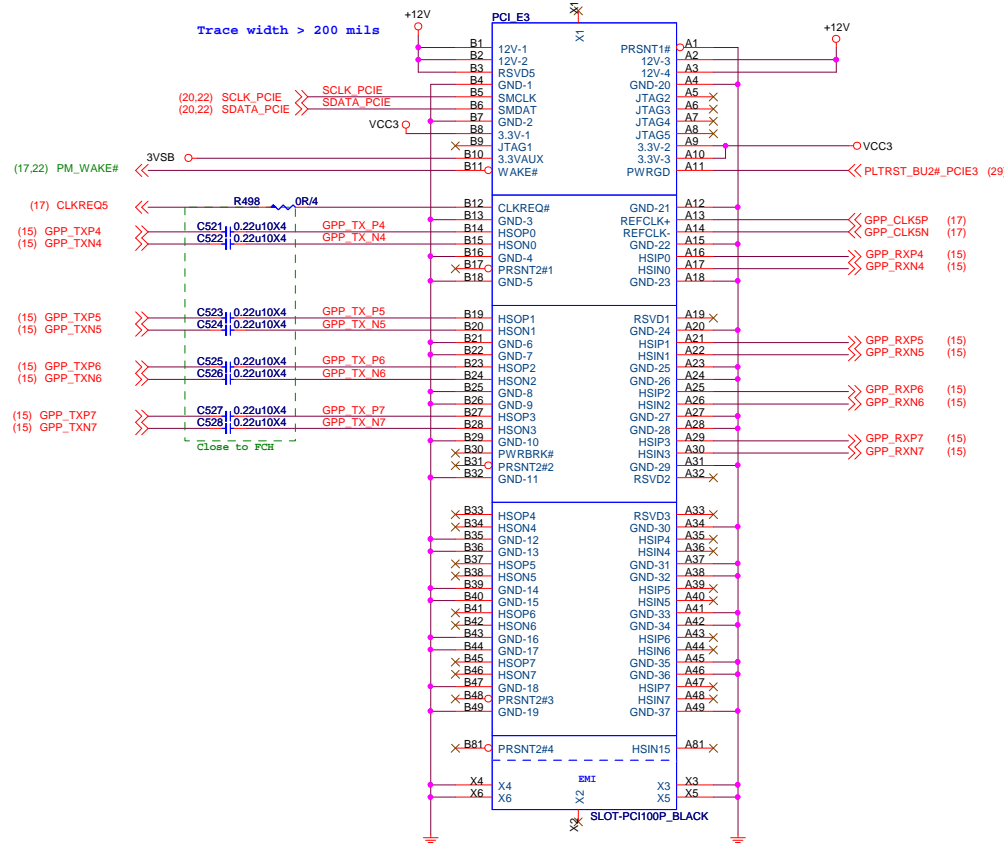
0.1u25X4

+12V		- 5.5A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA



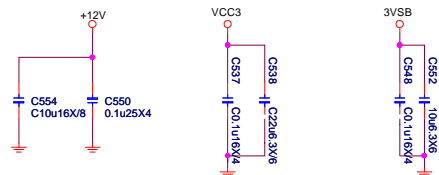
Size Custom	Document Description PCI_E1 (X16)	Rev 3.1
Date: Monday, May 06, 2019		Sheet 20 of 75

PCI_E3 X4

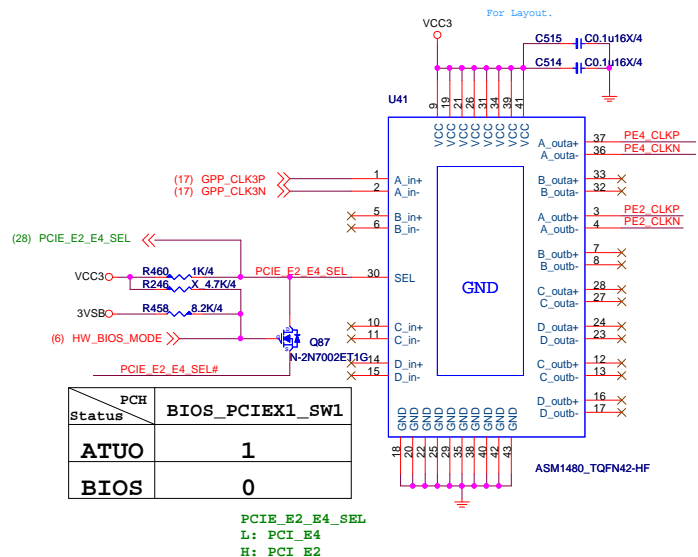


Vinafix.com

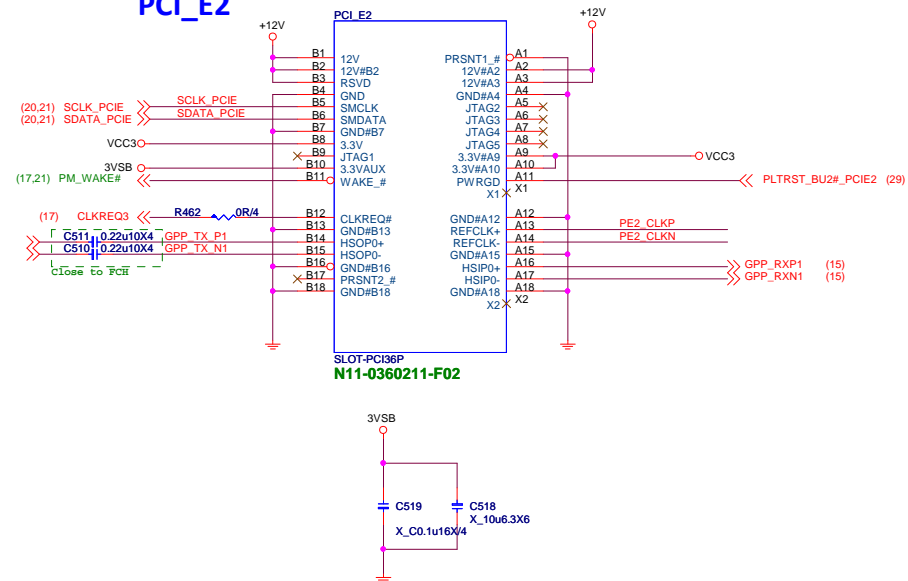
PCI Express x4 Slot *1		
+12V		- 2.1A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA



MICRO-STAR INT'L CO.,LTD			
MS-7C37			
Size	Document Description	Rev	
Custom	PCI_E3 (X4)	3.1	
Date:	Monday, May 06, 2019	Sheet	21 of 75

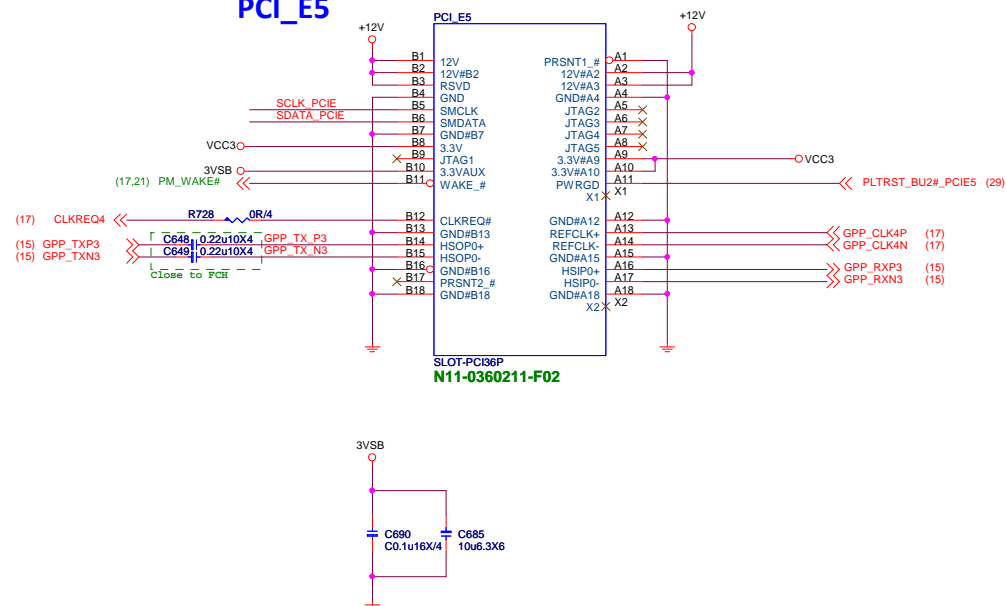


PCI_E2

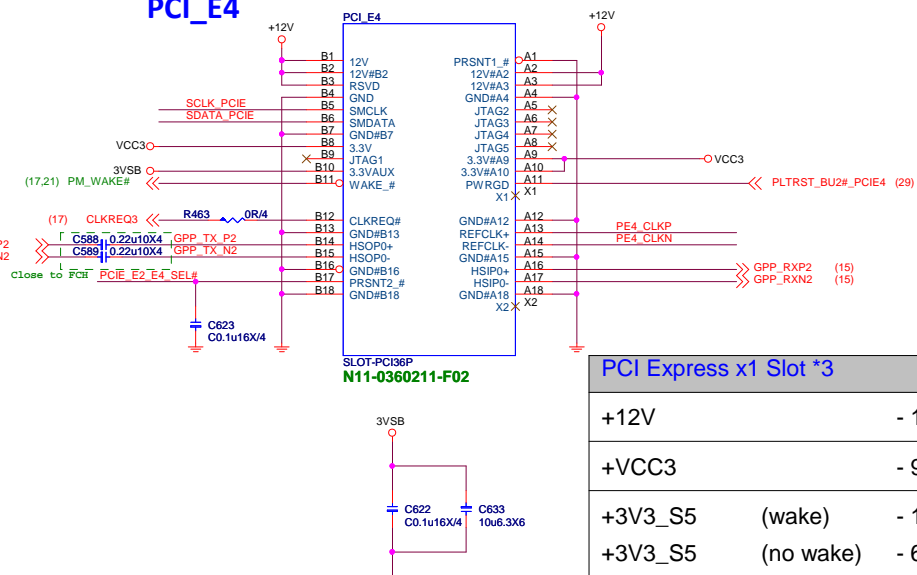


PCIE_E2 & PCIE_E4互切, PCIE_E2 & PCIE_E4同时有PCIE device 以PCIE_E4 优先

PCI_E5



PCI_E4



PCI Express x1 Slot *3

+12V	- 1.5 A
+VCC3	- 9A
+3V3_S5 (wake)	- 1125mA
+3V3_S5 (no wake)	- 60mA



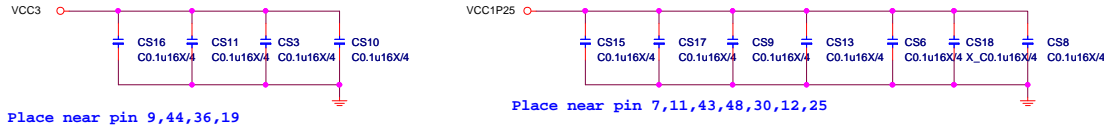
MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size Custom	Document Description	Rev 3.1
PCIE Switch PCI_E2 / E4 / E5 (X1)		
Date: Monday, May 06, 2019	Sheet 22	of 75

SATA Connector

1.2V delay from 3.3V 90% > 0ms

ASM1061 POWER Consumption

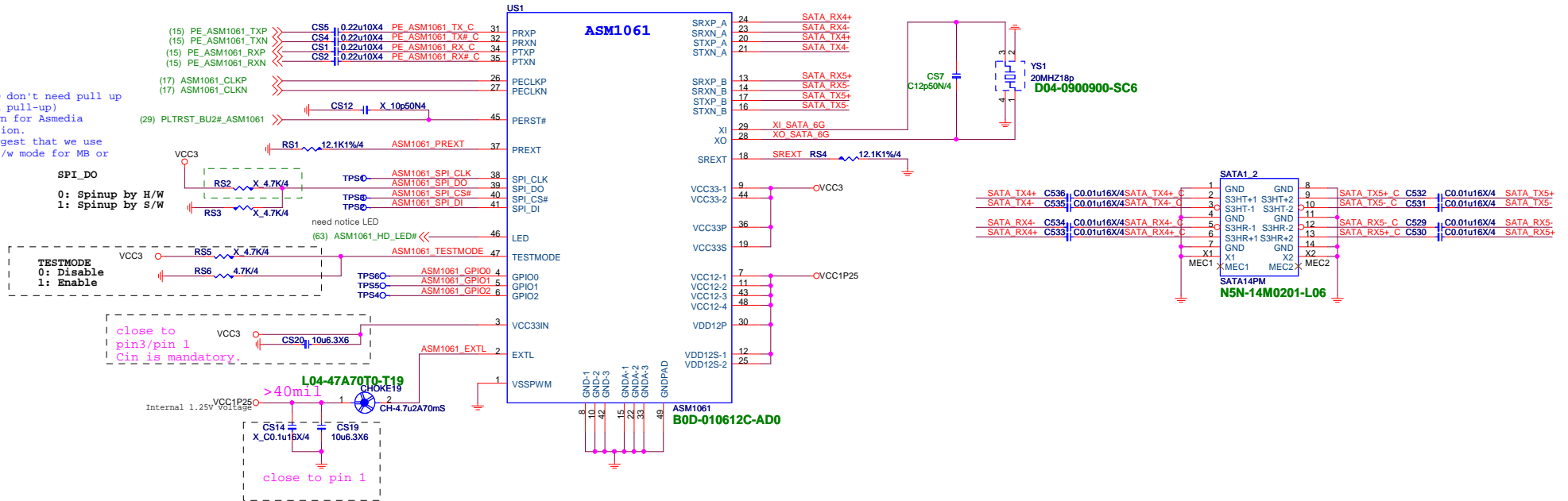
	3.3V	1.25V	Power (mW)
Idle (mA)	98.45	212.3	579.645
Busy (mA)	91.1	330.7	697.47

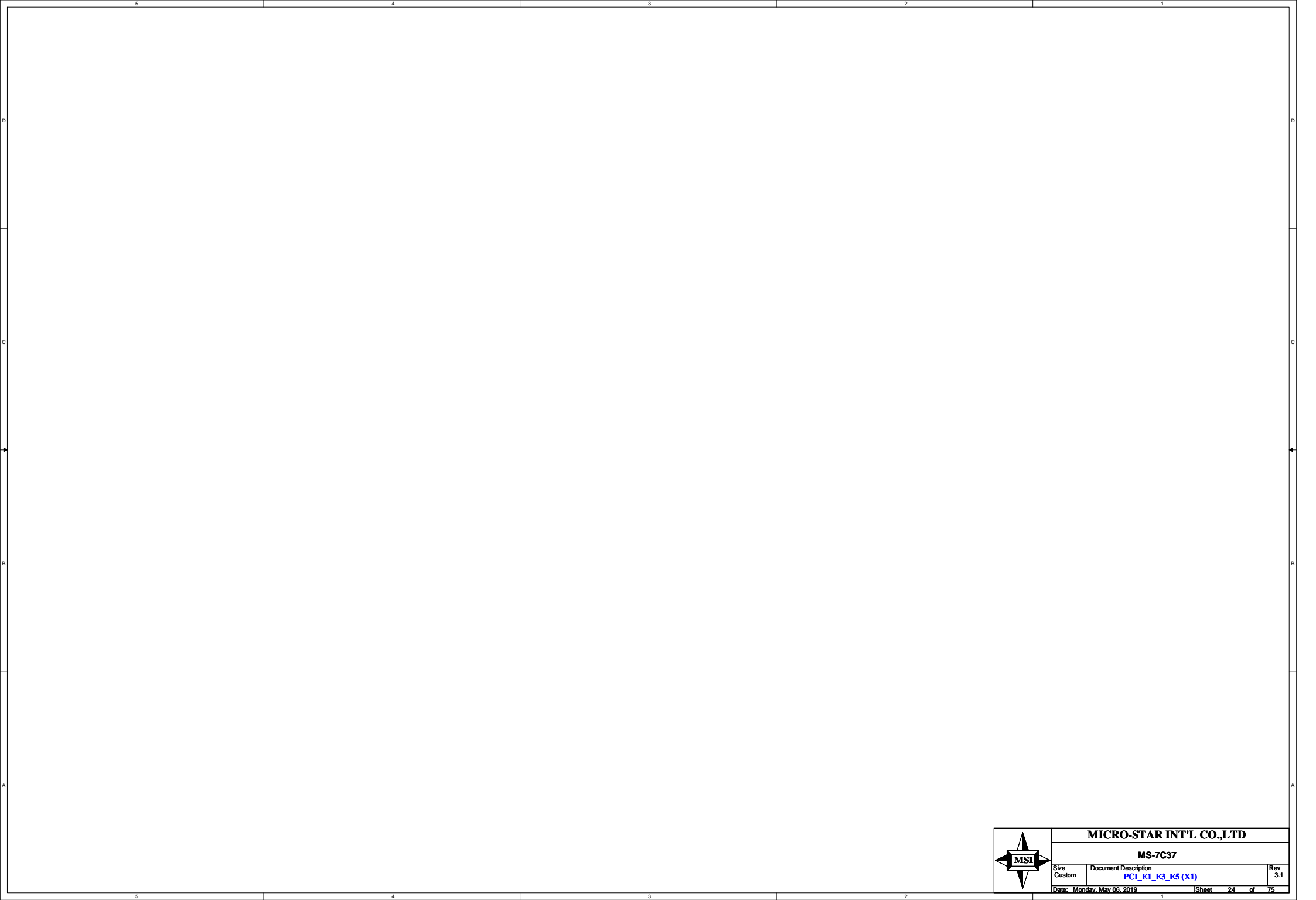


ASM1061 SATA6G

SATA_SPI_DO don't need pull up (integrated pull-up) or pull down for Asmedia recommendation.
Asmedia suggest that we use spinup by s/w mode for MB or PCI-E Card.

SPI_DO
0: Spinup by H/W
1: Spinup by S/W

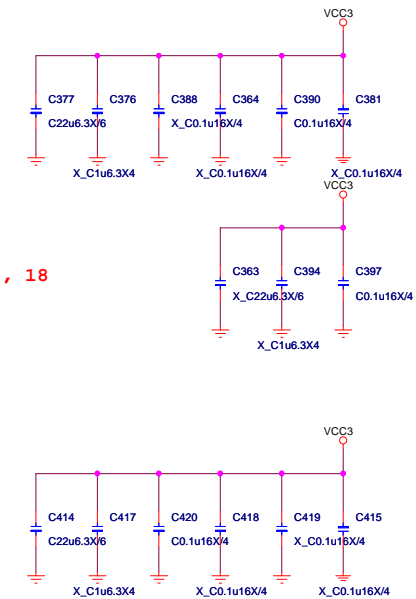
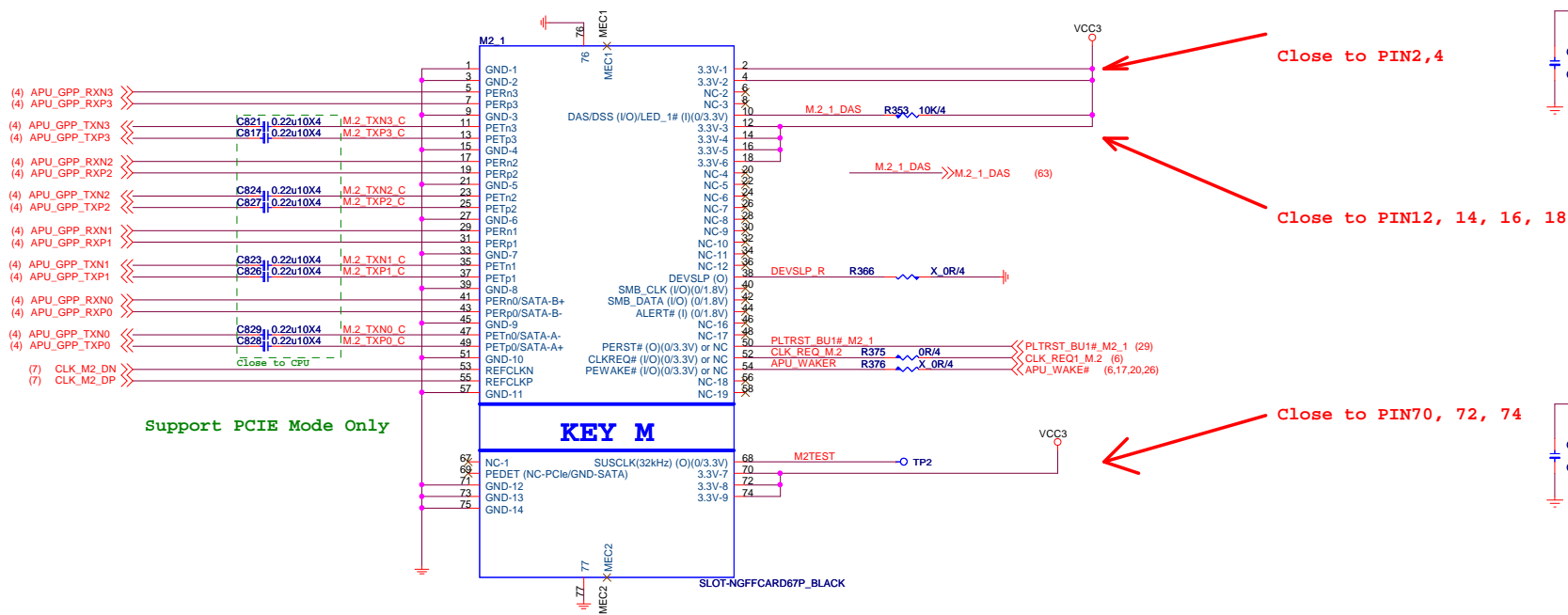




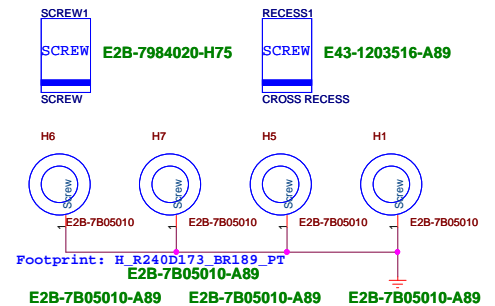
MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size Custom	Document Description PCI_E1_E3_E5 (X1)	Rev 3.1
Date: Monday, May 06, 2019		Sheet 24 of 75

M.2 1 Connector

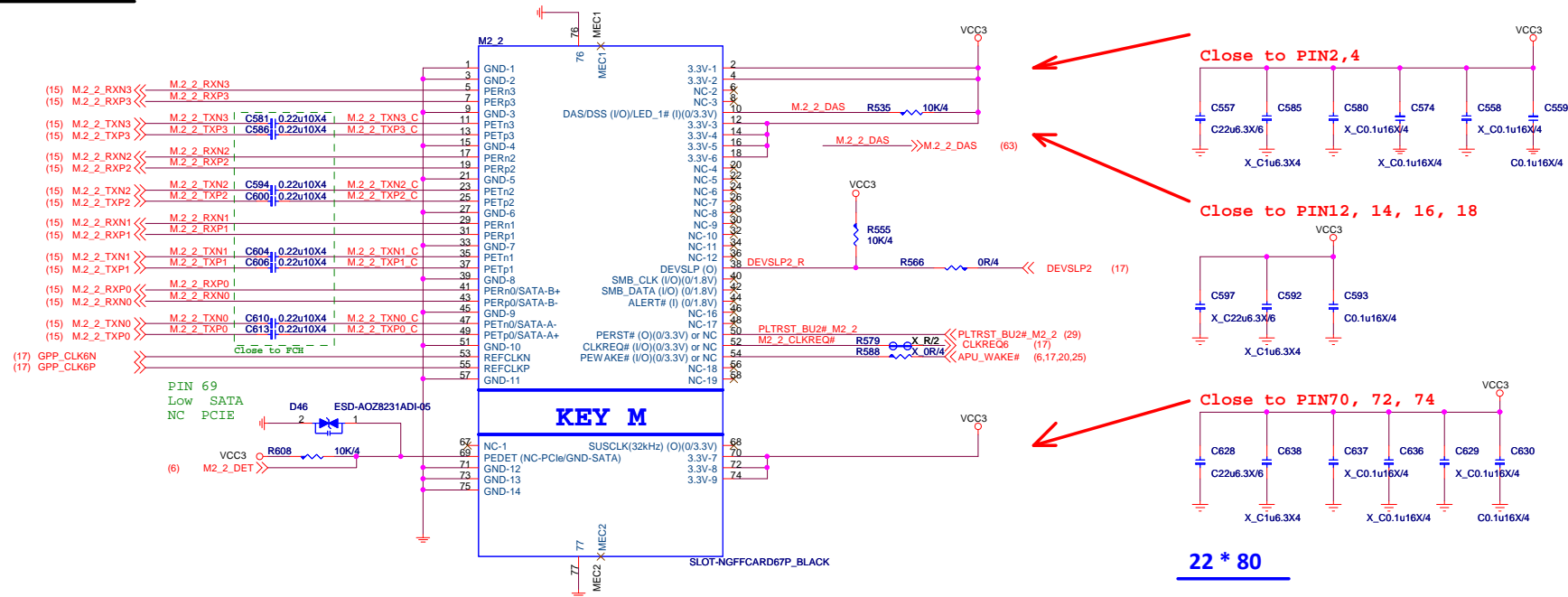
VCC3 4.25A
Max: 14W



22 * 110

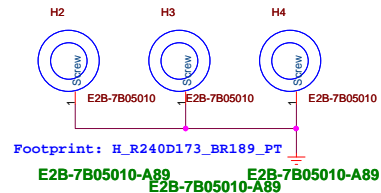
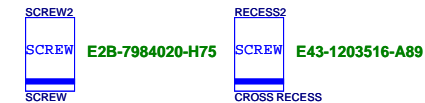


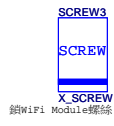
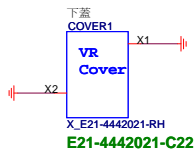
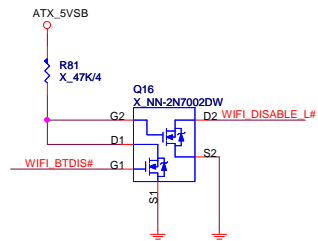
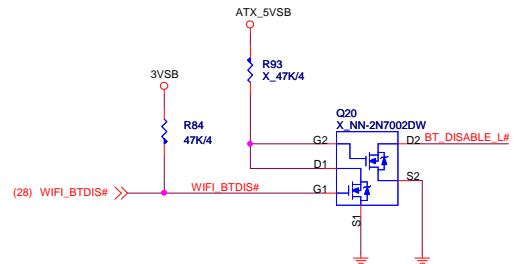
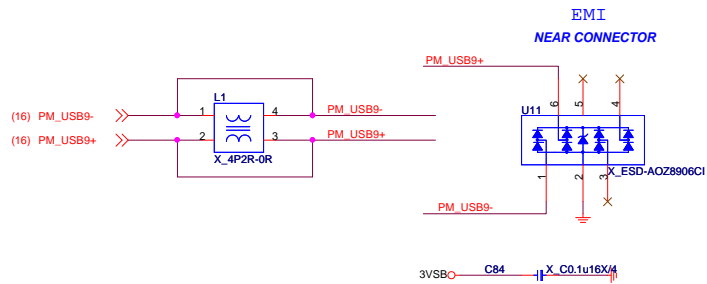
M.2 2 Connector



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22 * 80

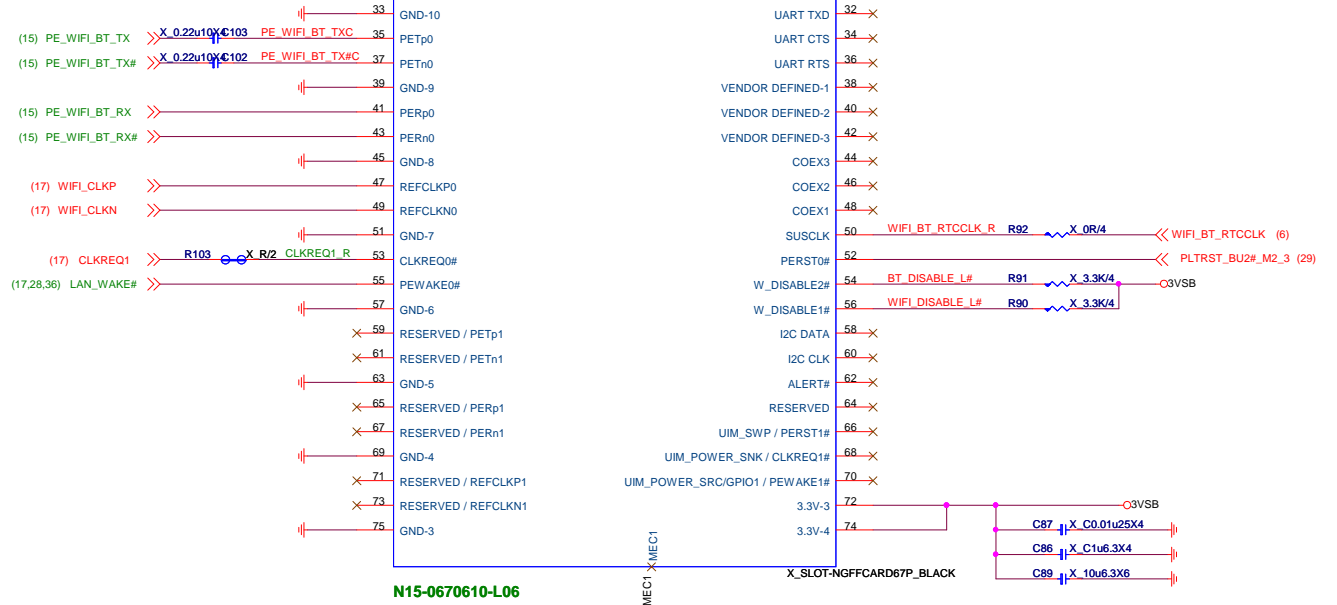




Wireless1
INTEL-3168
X_Wireless
604-4442-020

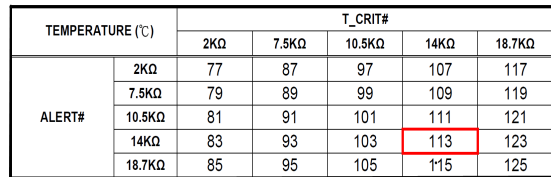
E43-1204046-P65

E43-1204046-P65



10uP+0.1uP+0.01uP at one end of socket in support of 3.3 V3V pins 2 and 4.
10uP+0.1uP+0.01uP at the other end of the socket in support of 3.3 V3V pins 70 and 72.

SIO HM Voltage over 2.048V will not detect



For System

W
Q90
B
C
C564
C2200p50X/4
GNDHM
SYSTIN
HM_VREF
R513
10K1%/4
RT4
10K1%/4
C5C3
C2200p50X/4
CPUMOSTIN
GNDHM

Close to CPU MOS

Schematic diagram of the PLTRST_BU2# signal path. The signal is generated by a NAND gate U72 (NC7SZ08M5X). The inputs to U72 are PM_PLTRST_BU2#_R (via R846, 4.7K/4), PM_PLTRST_BU2#_R (via R845, X_0R/4), and PM_GPP_RST (via R825, 0R/4). The output of U72 is PLTRST_BU2#. The signal path is also shown as a bus connection from SIO (28) PLTRST_BU2#_R to PLTRST_BU2#_LAN (36) and PLTRST_BU2#_ASM1061 (23).

I31-7116S09-N03

U46
GS7116SS-SOT23-5

ATX_5VSB

C541
10µF/6.3V

EN:VIH1.6V

3VA

C551
10µF/6.3V

R497
10K/4%

R488
3.16K/4%

3VA_FB

SIO_3VA

Vout = Vref * (1 + (R1/R2))
= 0.8 * (1 + (10K/3.16K))
= 3.33V

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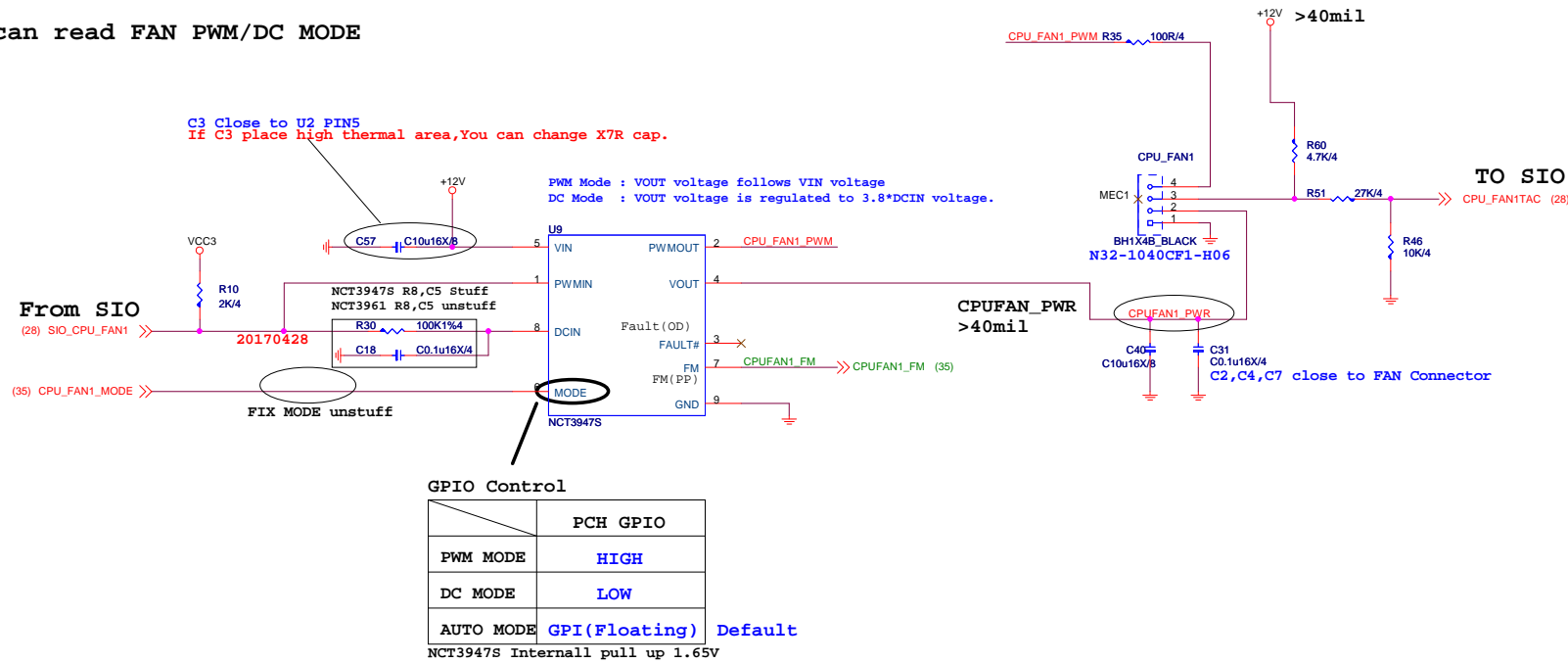
MS-7C37

Size Custom	Document Description SIO - HW Monitor / NCT7718W	Rev 3.1
Date: Monday, May 06, 2019		Sheet 29 of 75

TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

CPUFAN1

- 1.Mode GPIO BIOS can swtich PWM/DC MODE
- 2.FM:BIOS can read FAN PWM/DC MODE



PUMPFAN1

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO	
PWM MODE	HIGH	
DC MODE	LOW	
AUTO MODE	GPI(Floating)	Default

NCT3947S Internal pull up 1.65V



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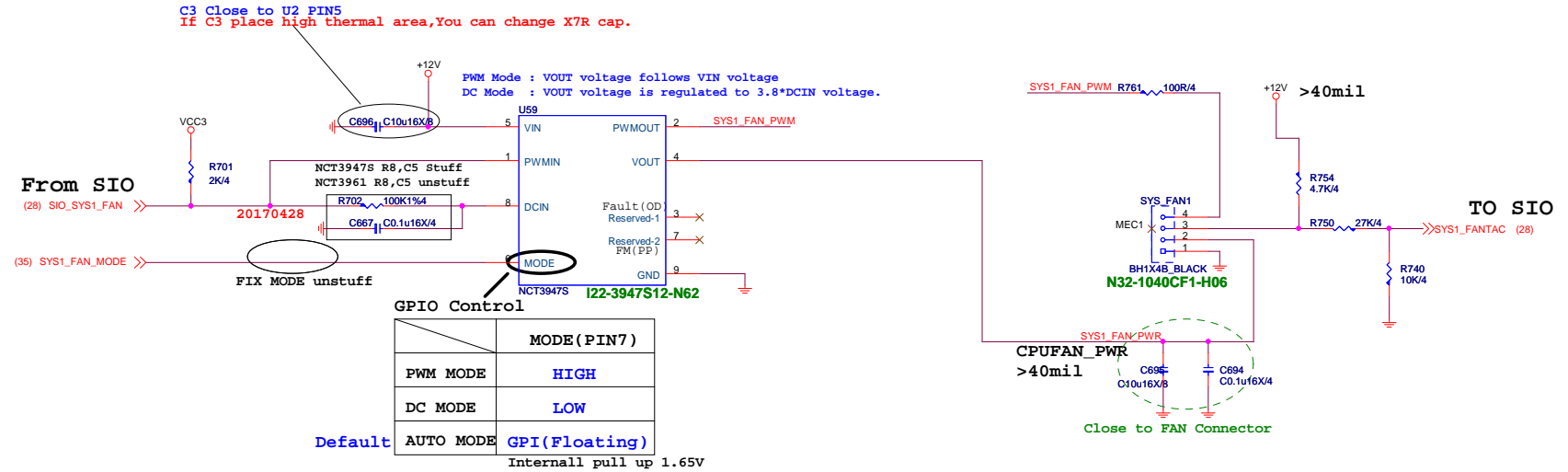
MS-7C37

Size Custom	Document Description FAN TYPE-K PUMPFANI	Rev 3.1
Date: Monday, May 06, 2019	Sheet 31 of 75	

SYSFAN1

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

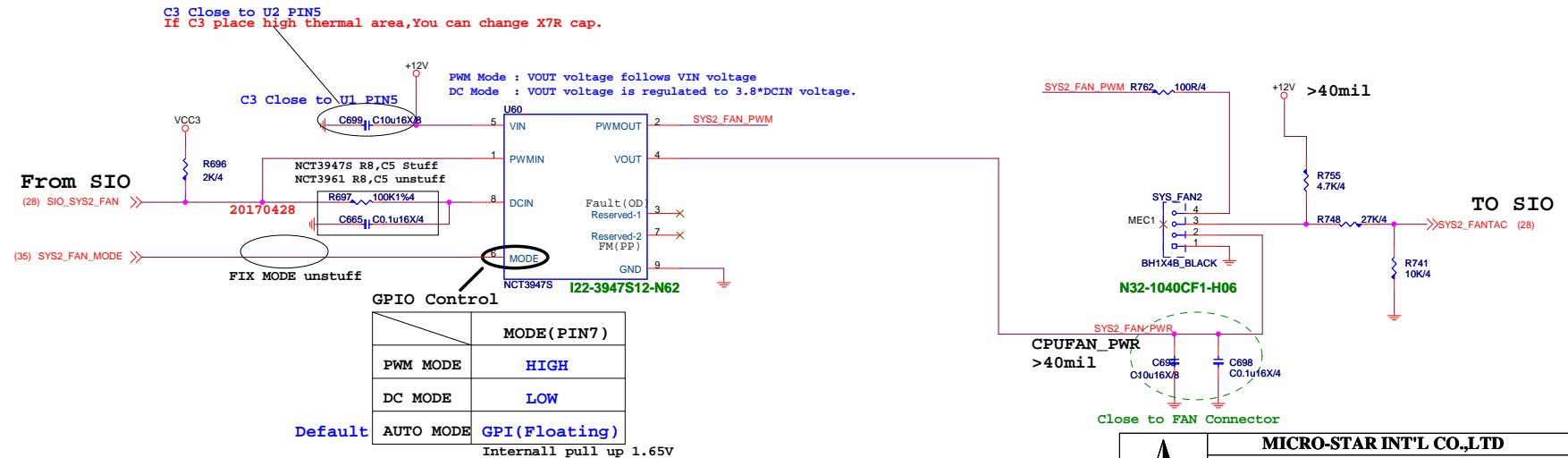
1.Mode GPIO BIOS can switch PWM/DC MODE



SYSFAN2

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can switch PWM/DC MODE



MICRO-STAR INT'L CO.,LTD

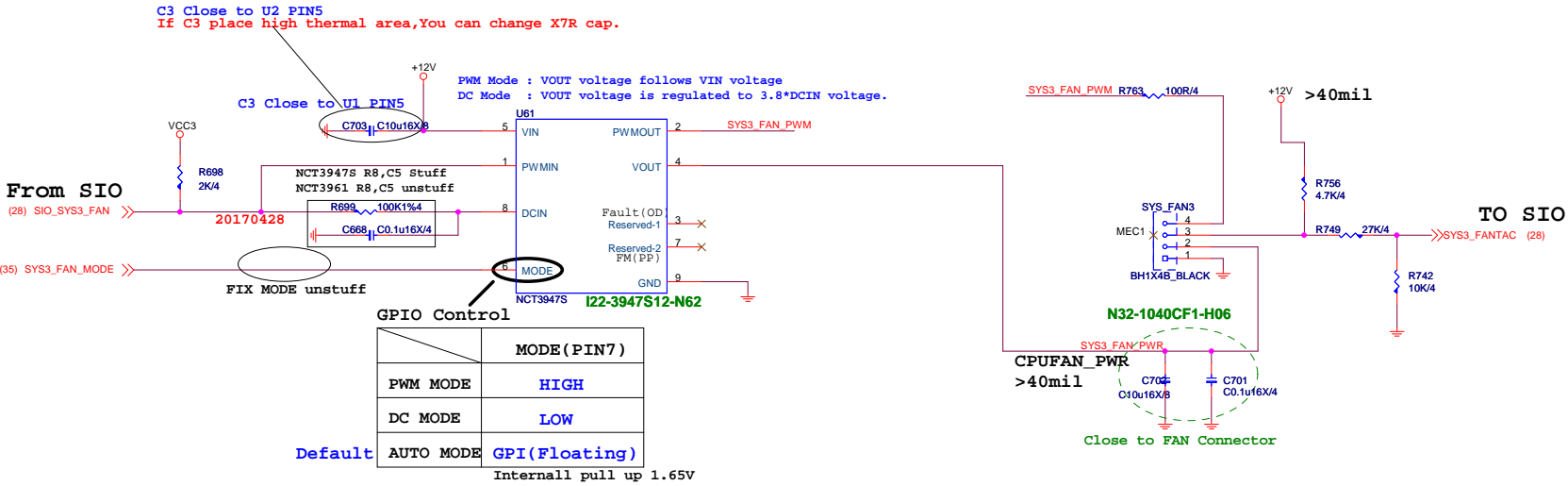
MS-7C37

Size	Document Description	Rev
Custom	FAN TYPE-K SYSFAN1/2	3.1
Date: Monday, May 06, 2019 Sheet 32 of 75		

SYSFAN3

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

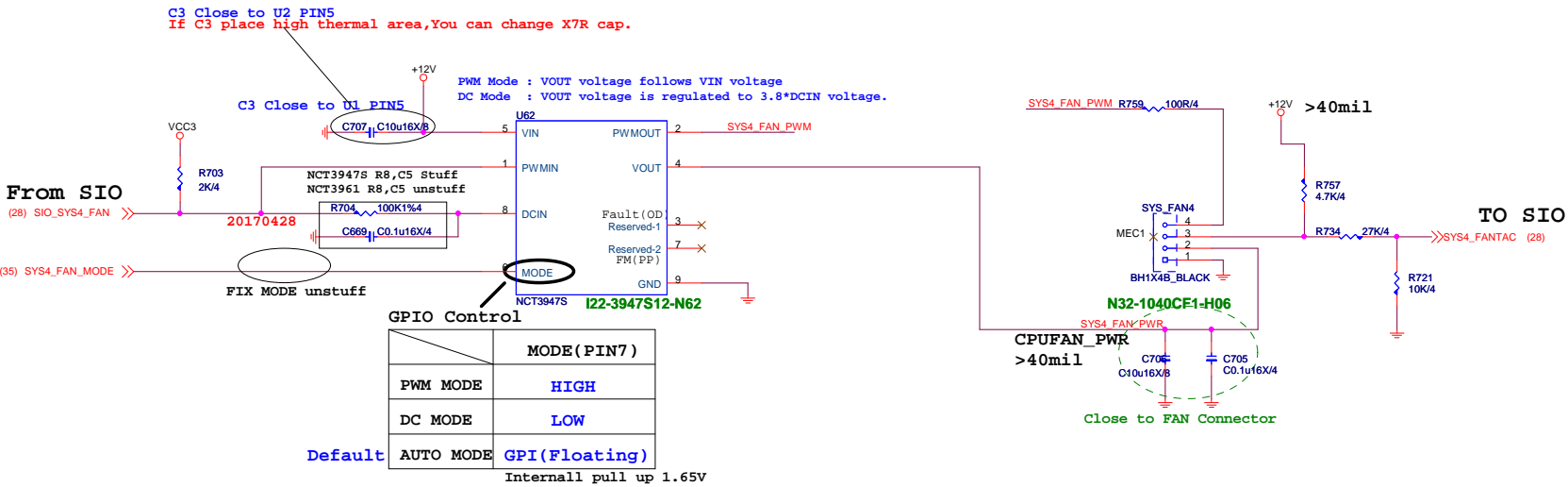
1.Mode GPIO BIOS can switch PWM/DC MODE



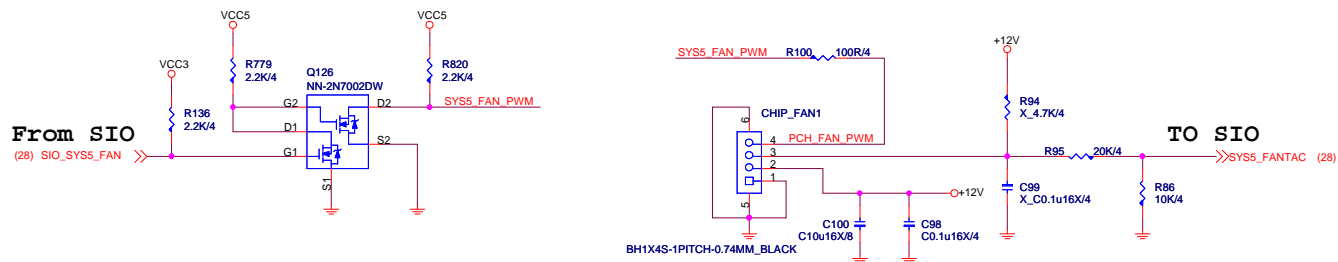
SYSFAN4

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can switch PWM/DC MODE



PCH_FAN



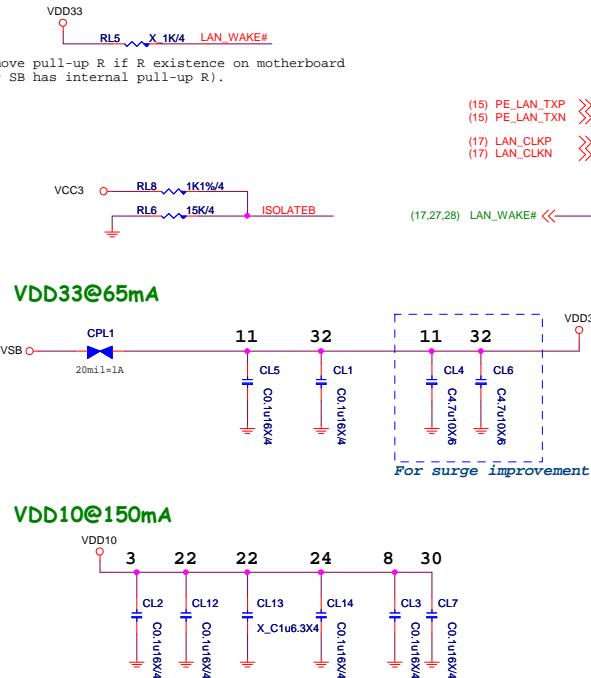
MICRO-STAR INT'L CO.,LTD

MS-7C37

Size Custom	Document Description PCH_FAN	Rev 3.1
Date: Monday, May 06, 2019		
Sheet 34 of 75		

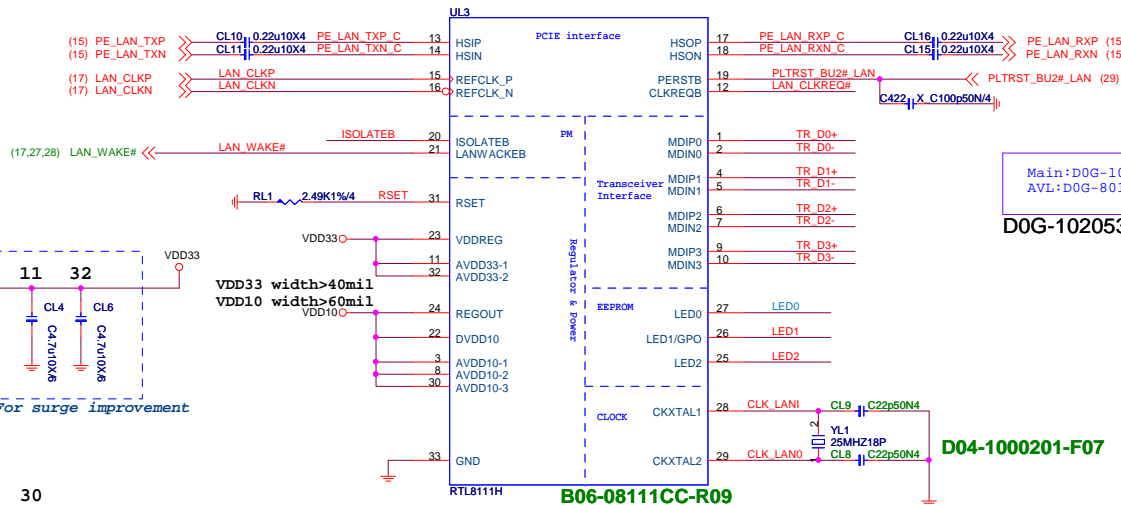
RTL8111H Giga LAN

Remove pull-up R if R existence on motherboard
(or SB has internal pull-up R).



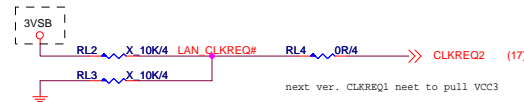
VDD10@150mA

VDD33@65mA



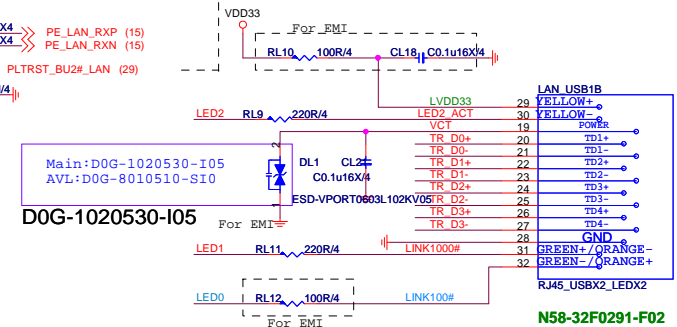
Pin33: 4 via from top layer to GND layer
and make the via at the center of IC.

Pull-up resistor RL9 required to either
3.3V suspend or core rail depending on
the power well of the PCH input CLKREQ# buffer.



PIN19:
AMD platform connect to PCIE_RST#,
don't connect to A-RST#.
INTEL platform connect to PLT_RST#,

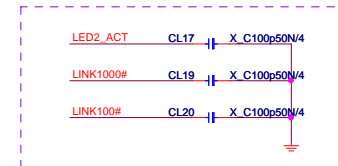
LAN Connector



N58-32F0291-F02

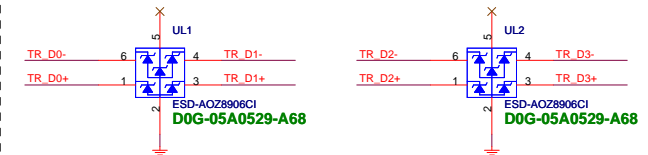
D04-1000201-F07

For EMI



ESD Protect
close to connector

D0G-0200529-A68
D0G-0100619-I05



8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

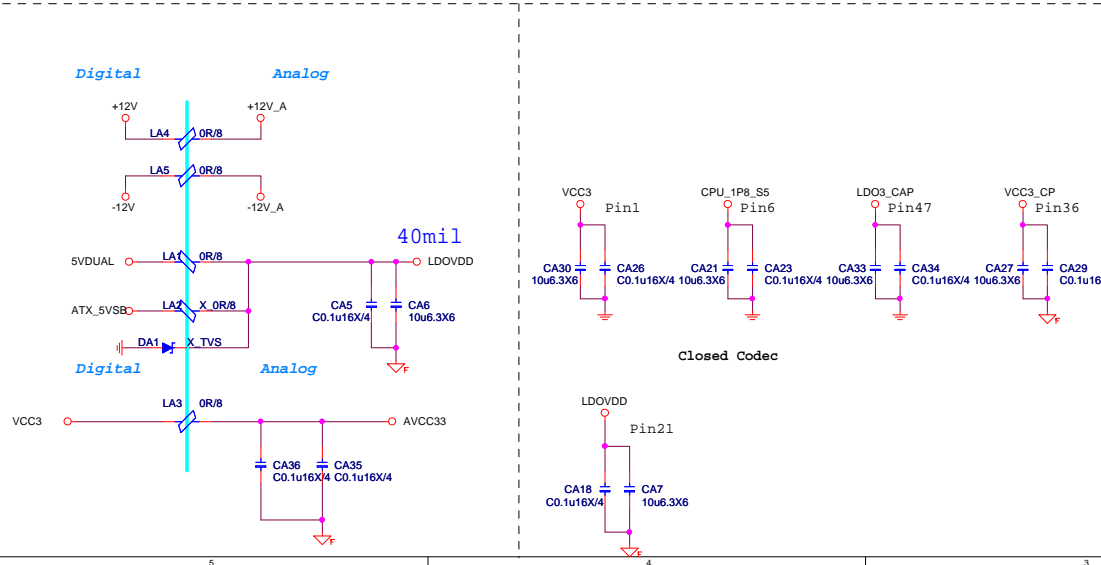
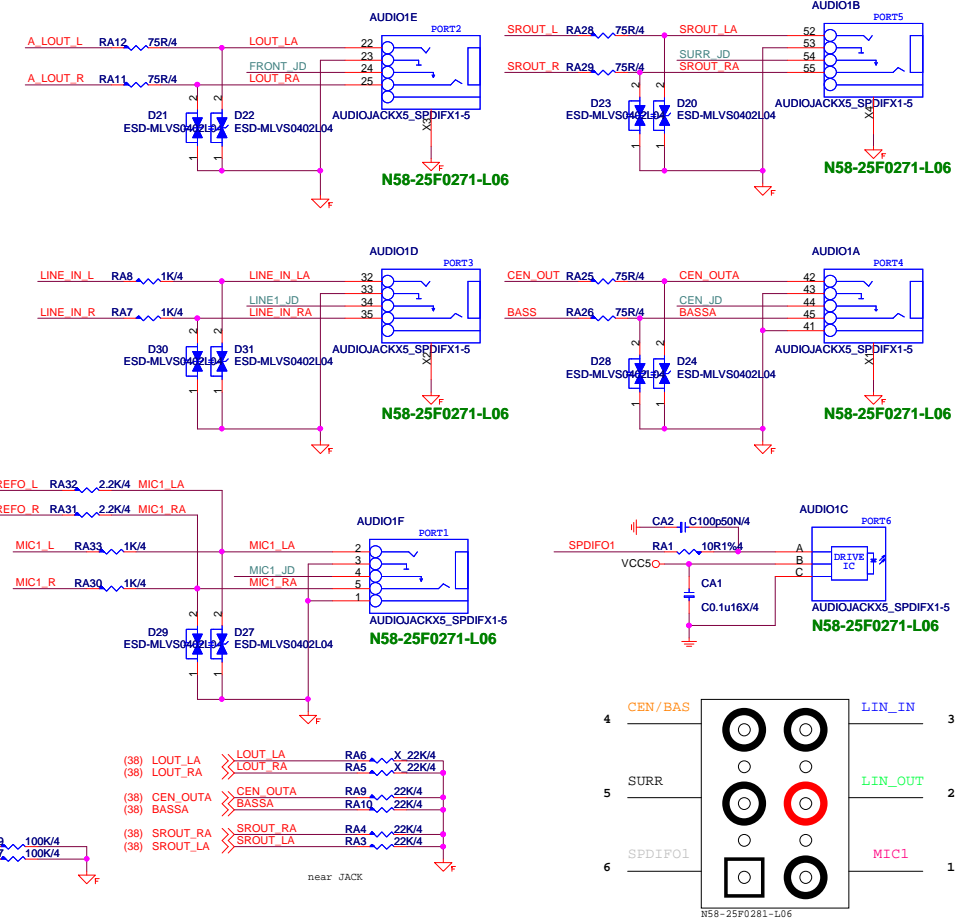
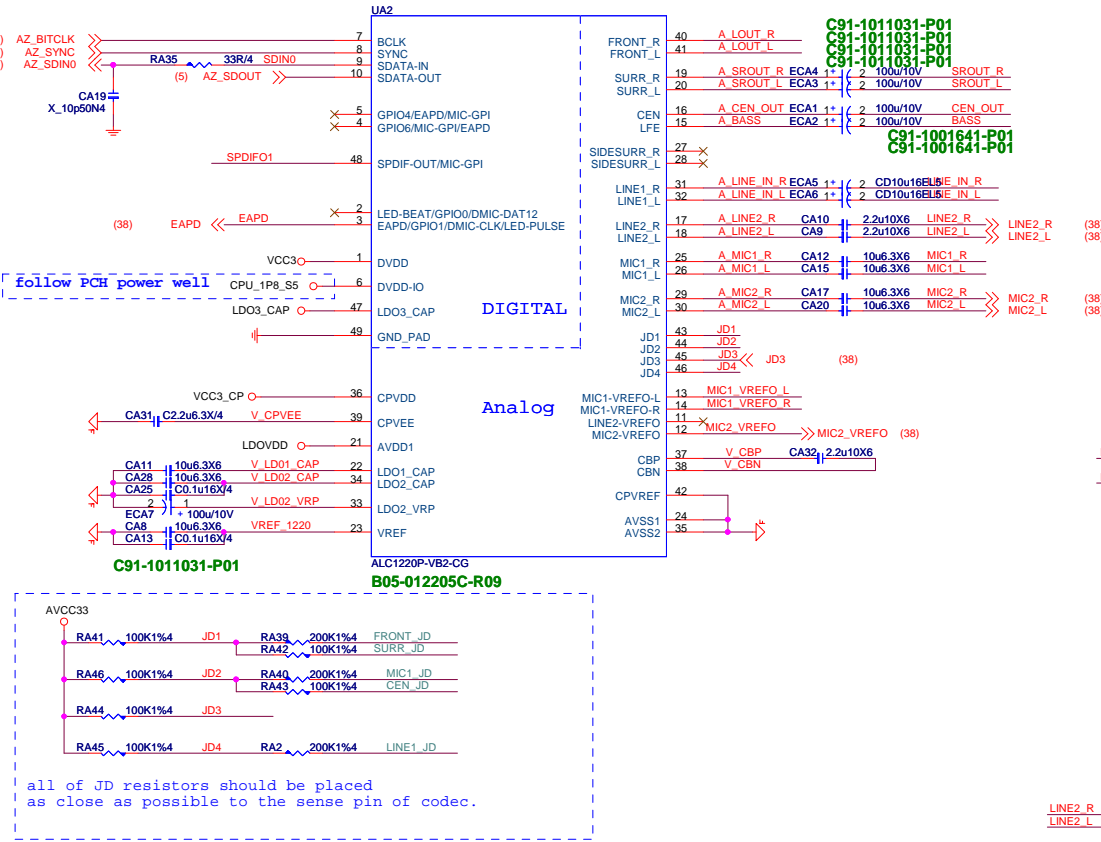


MICRO-STAR INT'L CO.,LTD

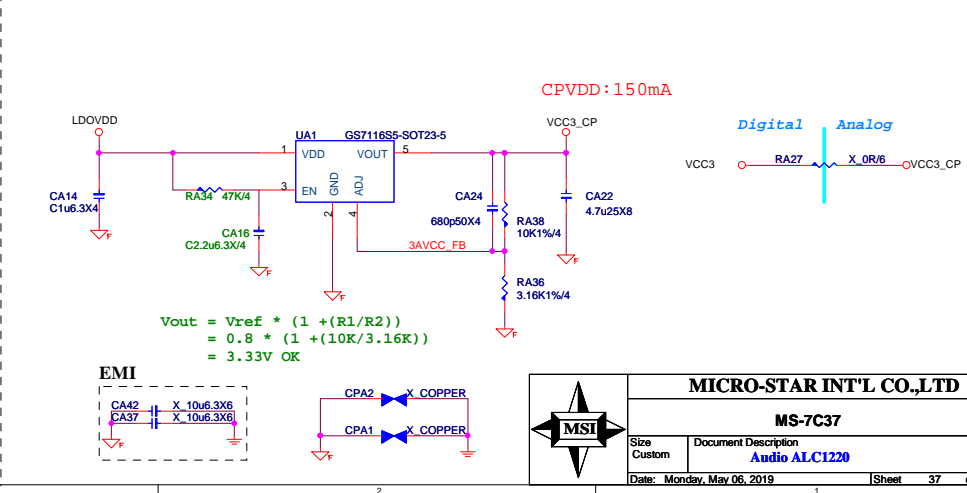
MS-7C37

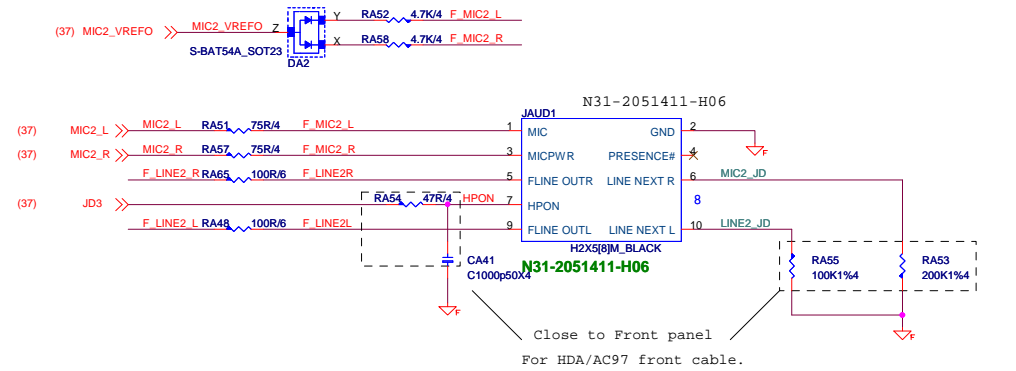
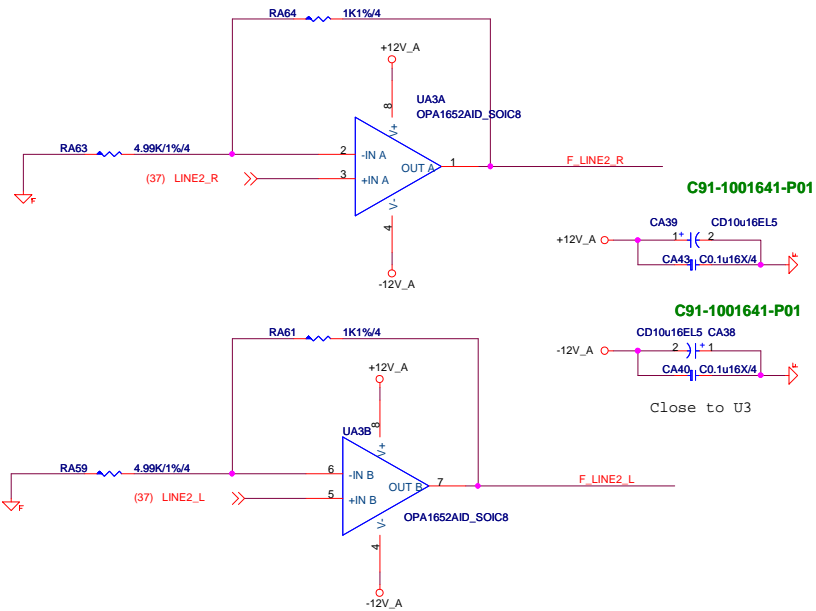
Size	Document Description	Rev
Custom	LAN - I211AT	3.1
Date: Monday, May 06, 2019	Sheet 36 of 75	

ALC1220P-VB2_48PIN



CPVDD POWER:ATX5VSB will Leakage to CVDD by ALC1220, so CVDD must keep 3.3V

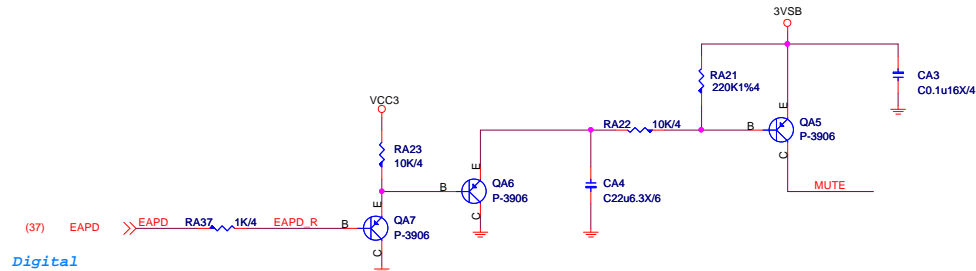




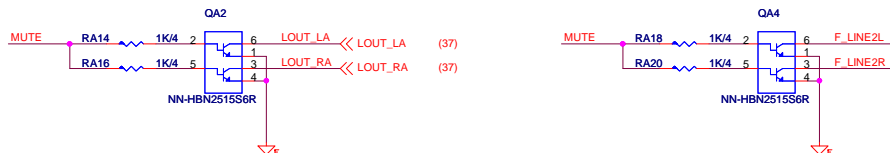
Close to Jack
ESD protect



Rear Line OUT De-POP circuit (De-pop circuit for Rear Line out & Front Headphone out)

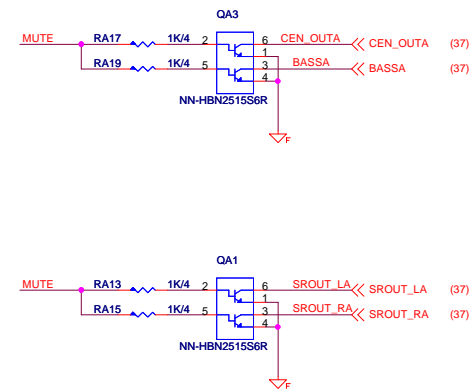


Analogue




Audio moat is transparent and width 40mil

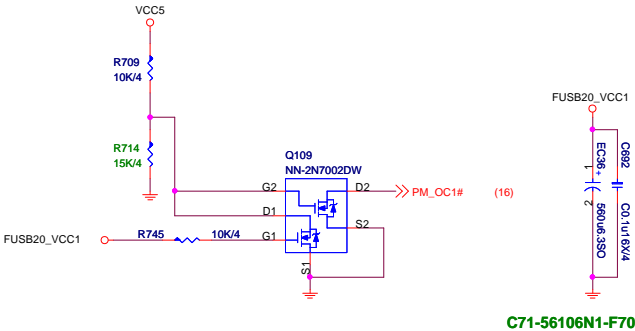
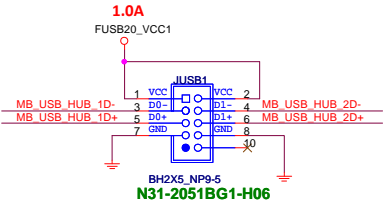
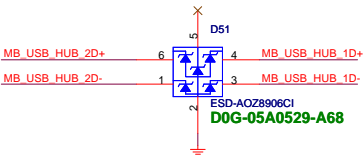
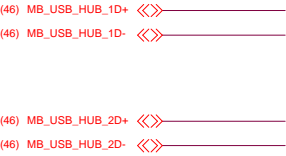
(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change SROUT_LA, SROUT_RA, CEN_OUTA, BASSA to TVS)



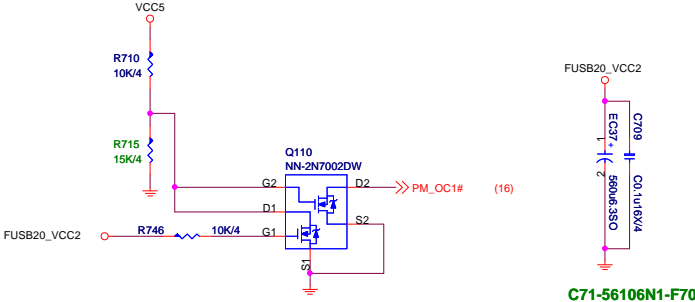
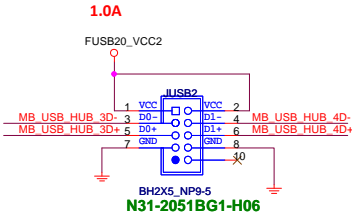
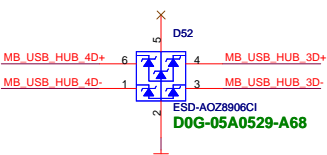
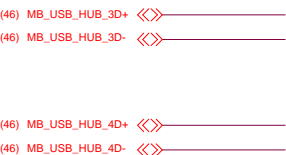
[illegible][illegible][illegible]

	MICRO-STAR INT'L CO.,LTD		
	MS-7C37		
	Size Custom	Document Description USB Power - UP7501	Rev. 3.1
	Date: Monday, May 06, 2019		Sheet 39 of 75

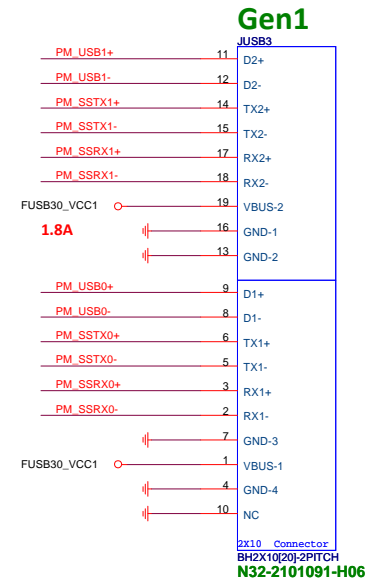
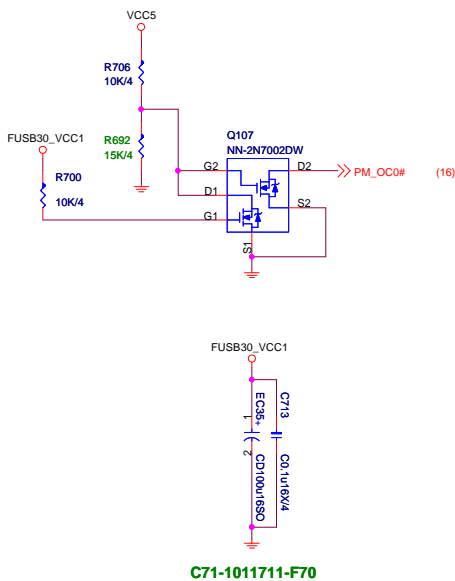
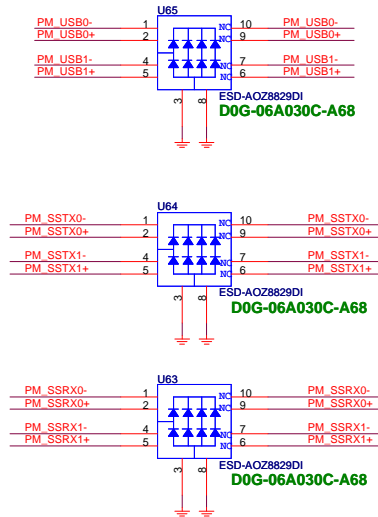
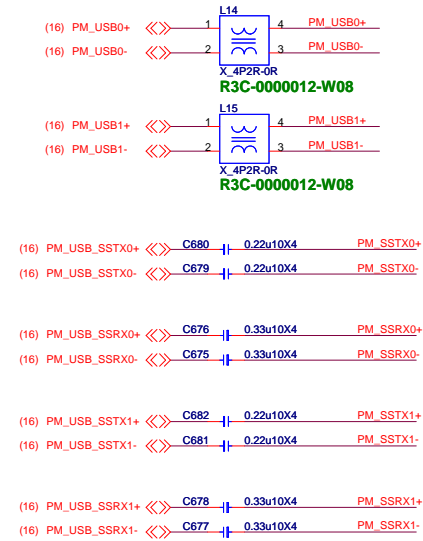
Front USB2.0(JUSB1)



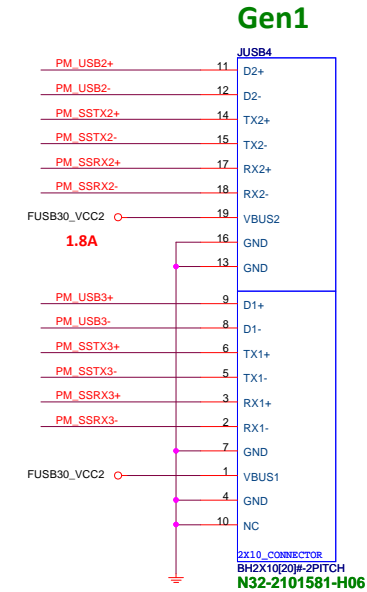
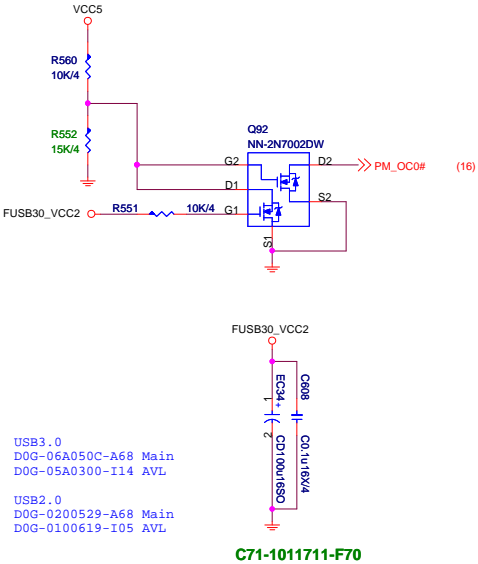
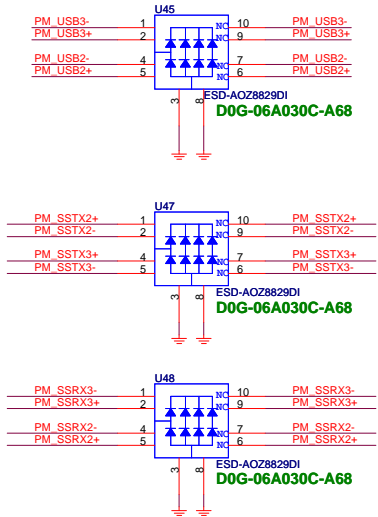
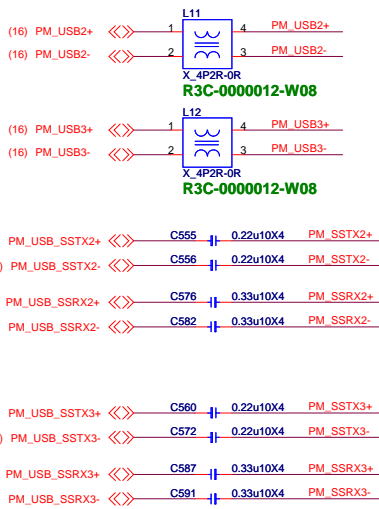
Front USB2.0(JUSB2)



Front USB3 180° BOX Header(JUSB3)



Front USB3 90° BOX Header(JUSB4)



PS2

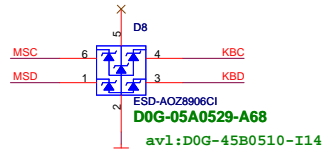
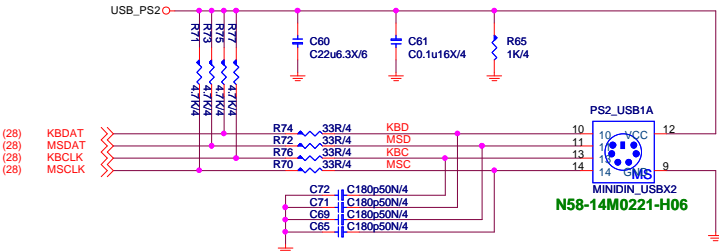
5V@1A

layout note:

C21 must close to TVS pin5

TVS must near KB_MS1 connector and route without branch

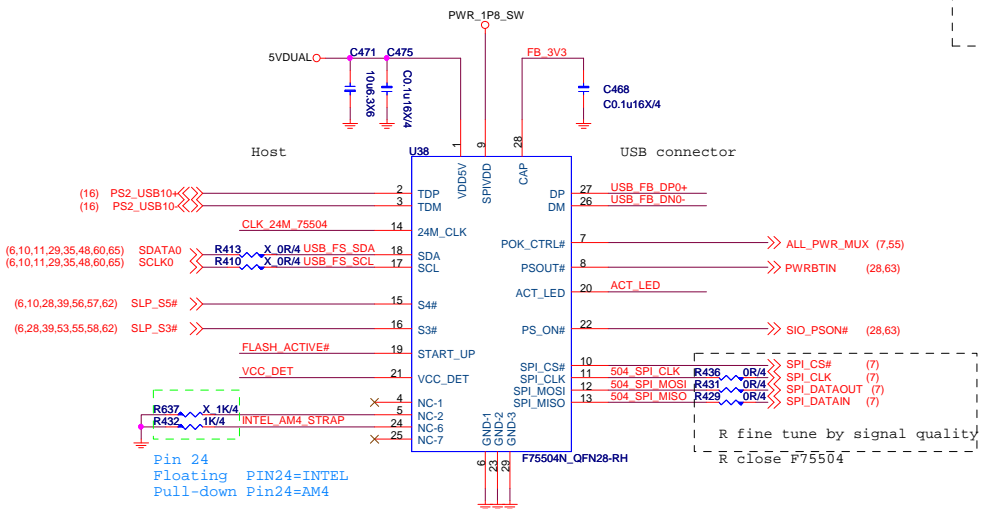
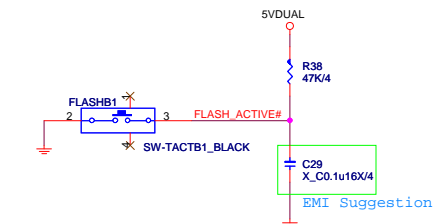
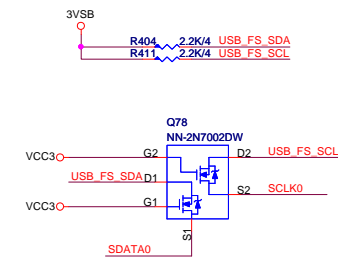
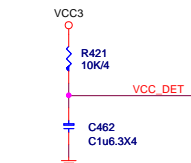
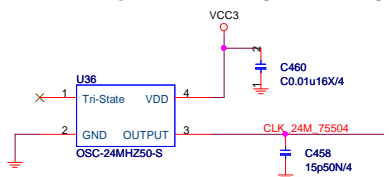
Varistor must close to TVS and route without branch



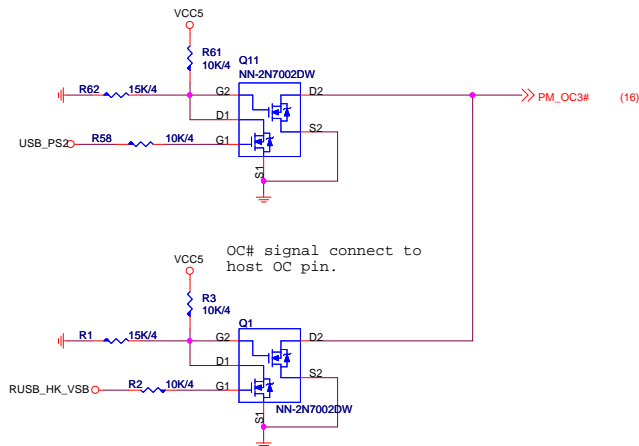
USB2.0 Flash BIOS

F75504 layout placement must meet to spi/usb trace length spec with host.
As for as possible place near to host.

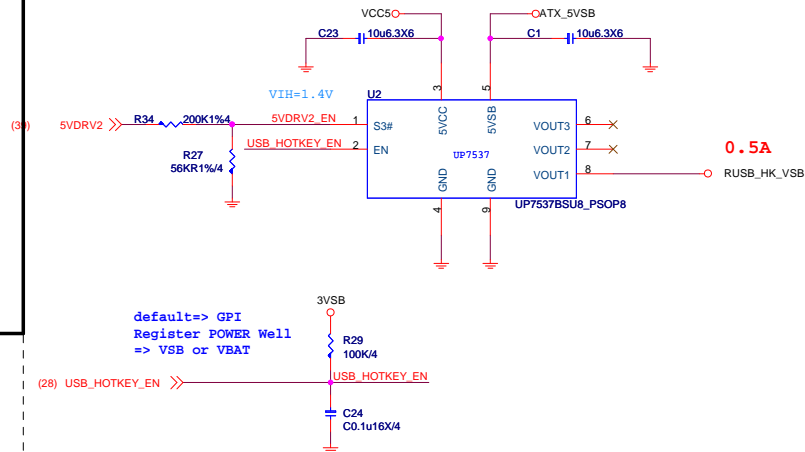
CLK running in S0,don't require in sleep



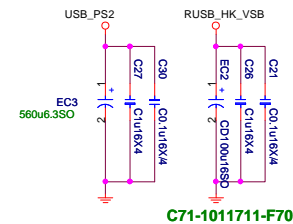
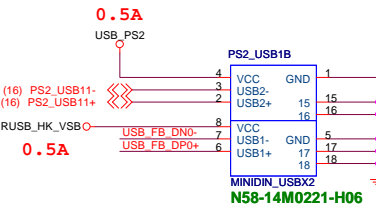
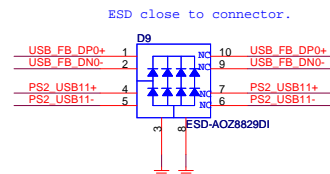
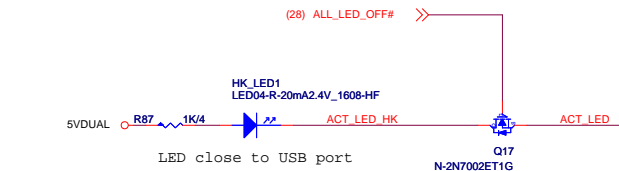
Pin 24
Floating PIN24=INTEL
Pull-down Pin24=AM4



HOTKEY POWER



default=> GPI
Register POWER Well
=> VSB or VBAT

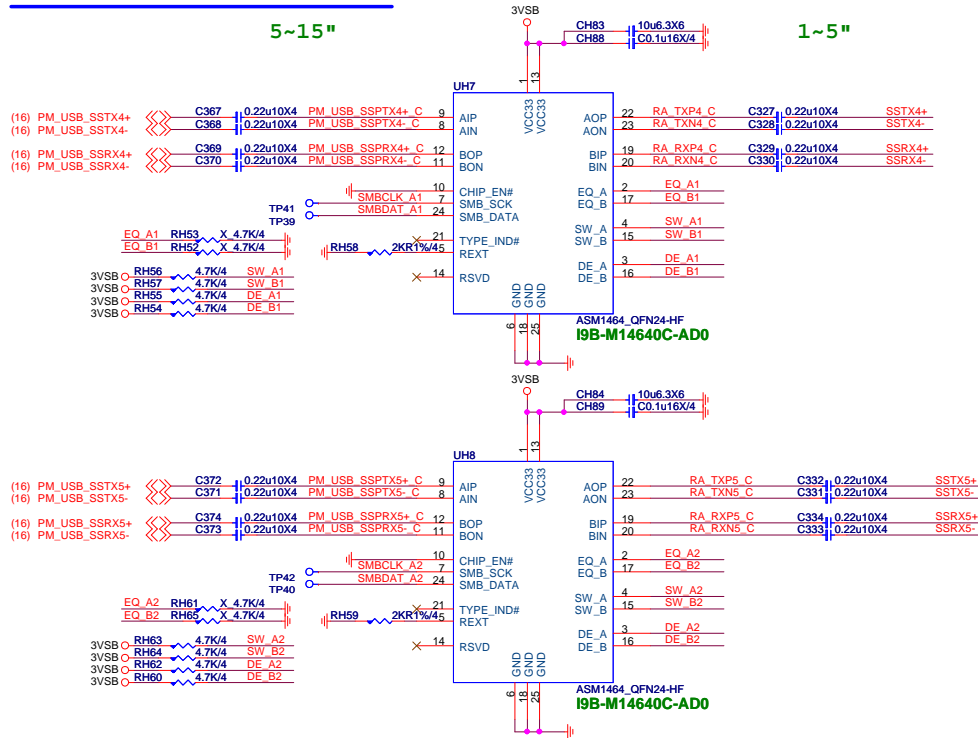


LAN USB3.1 Gen1 Type-A

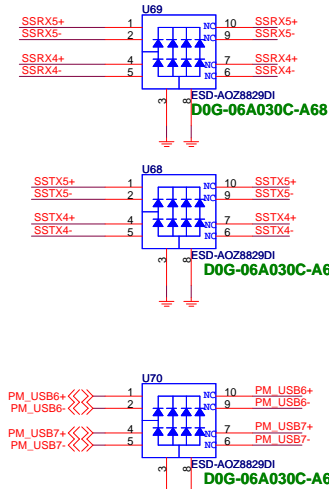
5~15"

0.13A

1~5"

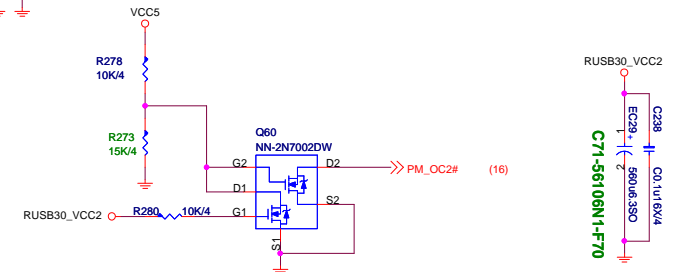
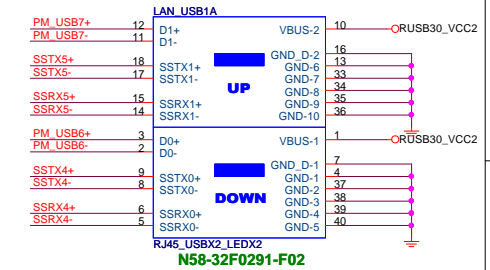


Rear LAN Type-A

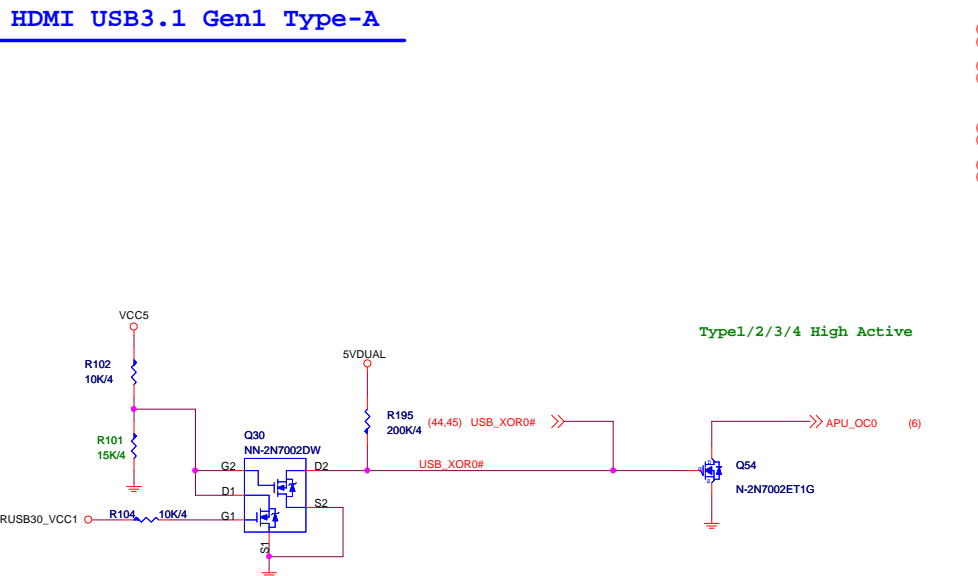


Gen1

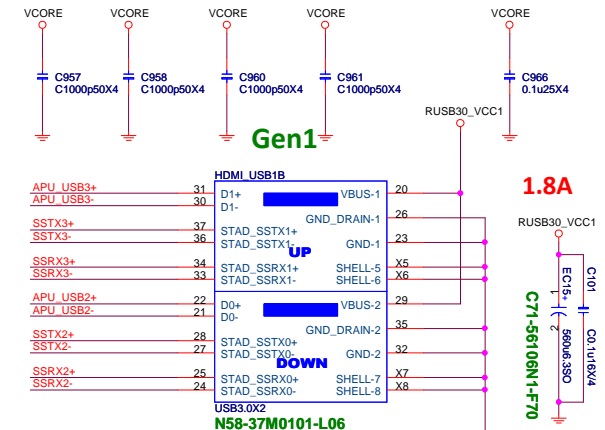
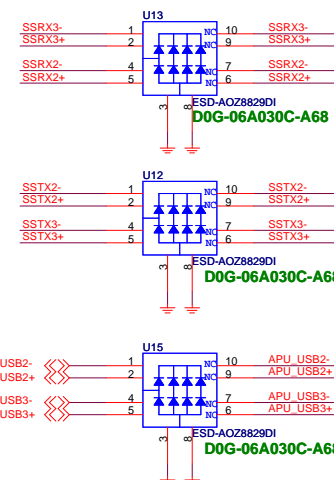
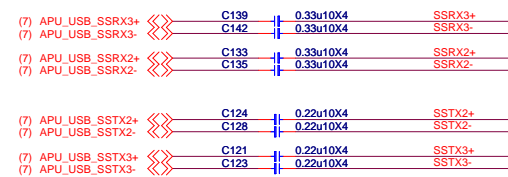
1.8A



HDMI USB3.1 Gen1 Type-A



Type1/2/3/4 High Active



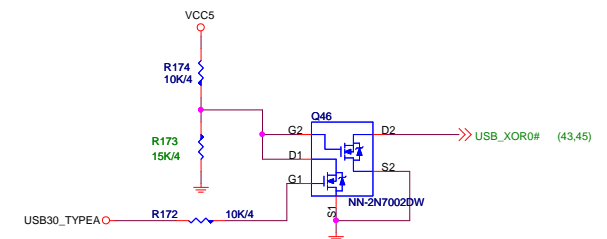
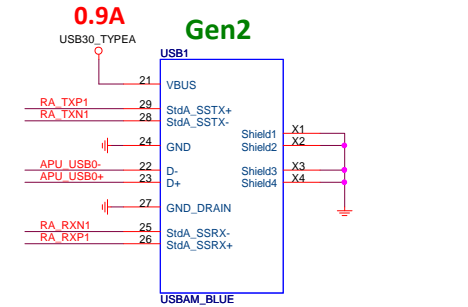
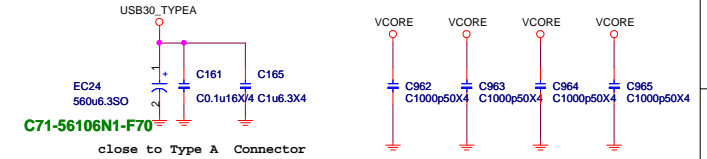
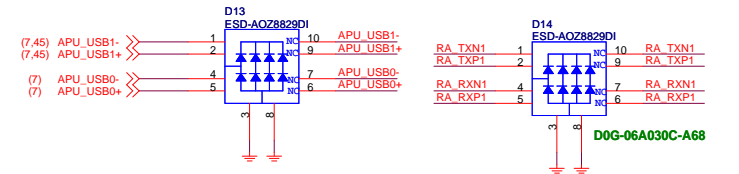
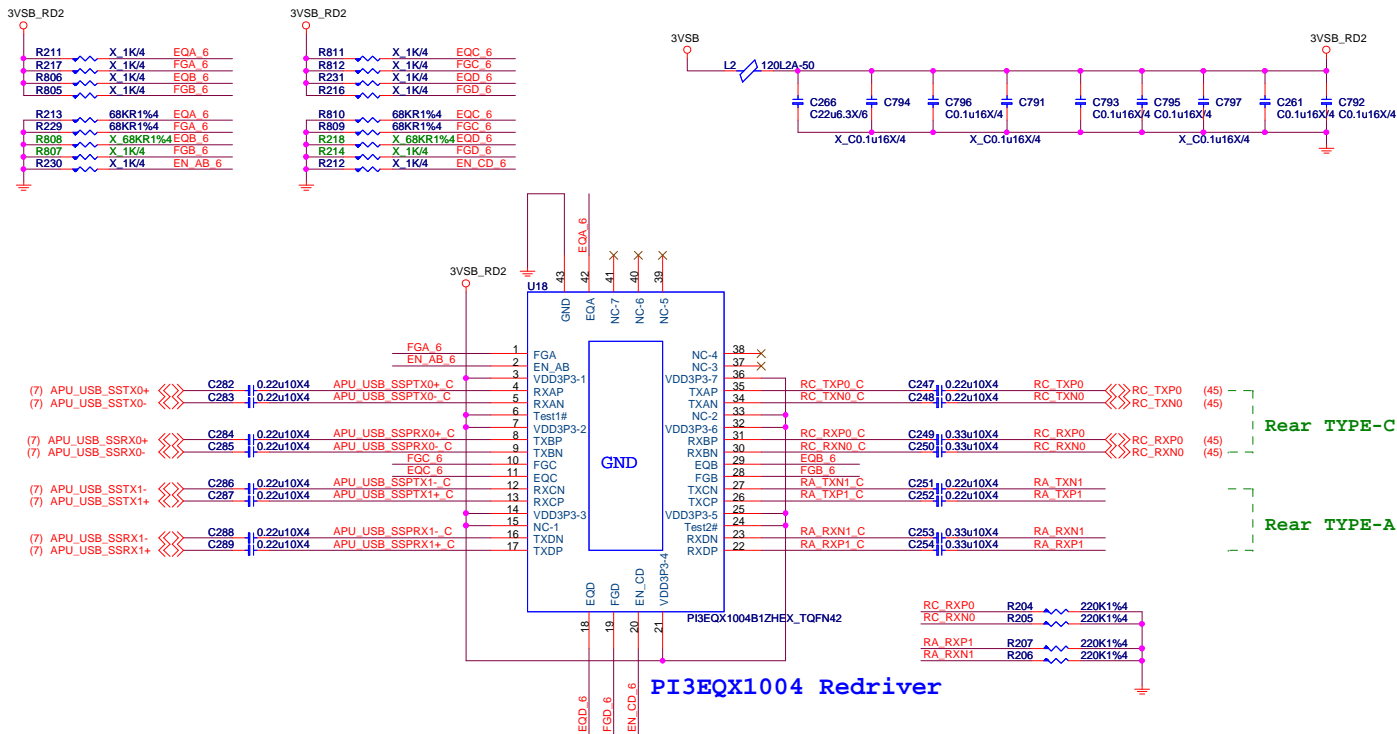
Gen1

1.8A

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MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size	Document Description	Rev
Custom	Rear_USB3.0 * 4	3.1
Date: Monday, May 06, 2019		
Sheet 43 of 75		

USB3.1 Gen2 Redriver + Type-A

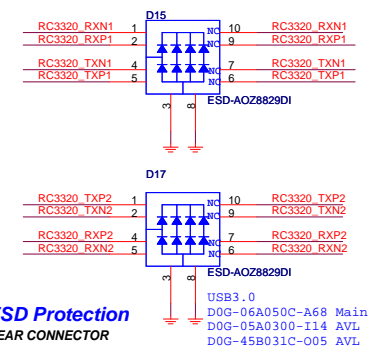
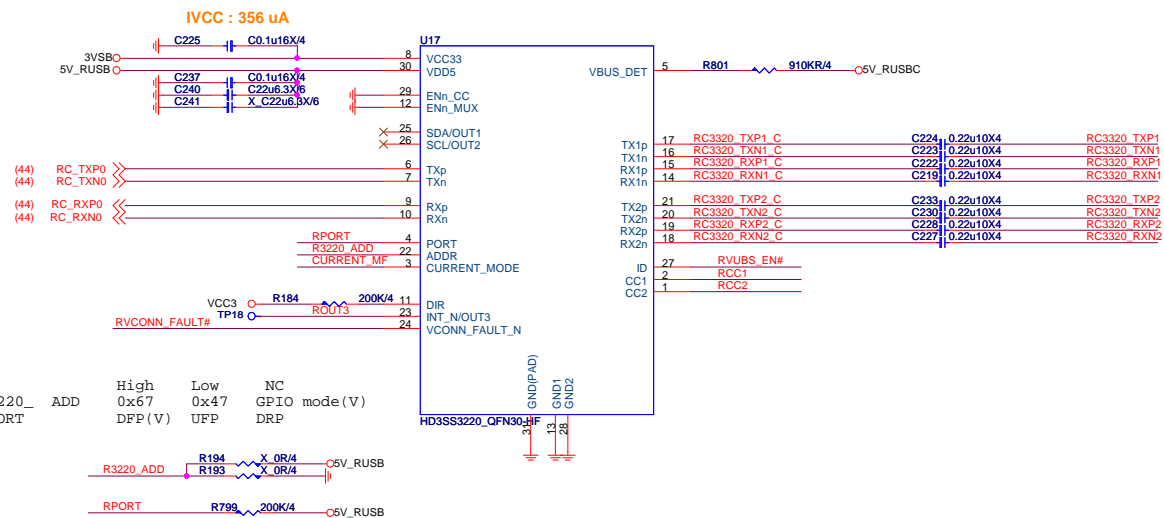


MICRO-STAR INT'L CO.,LTD

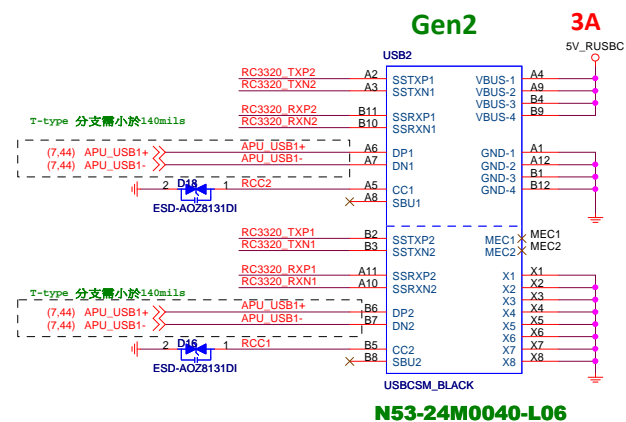
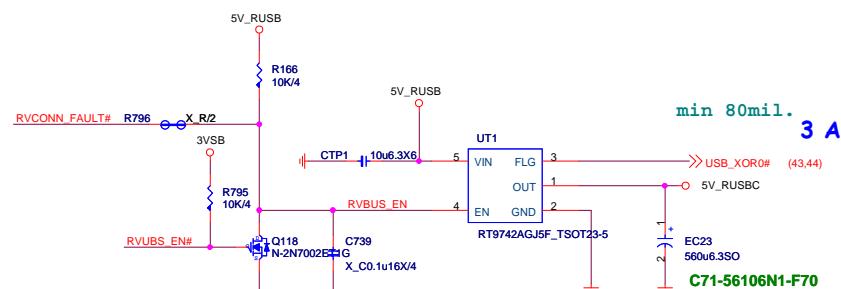
MS-7C37

Size Custom	Document Description Rear USB3.1 Type A / redrive	Rev 3.1
Date: Monday, May 06, 2019		Sheet 44 of 75

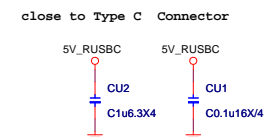
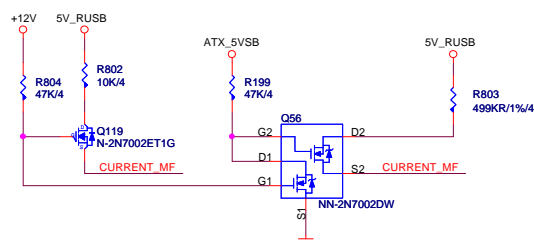
USB Type-C MUX with Configuration Channel (CC)



VBUS EN



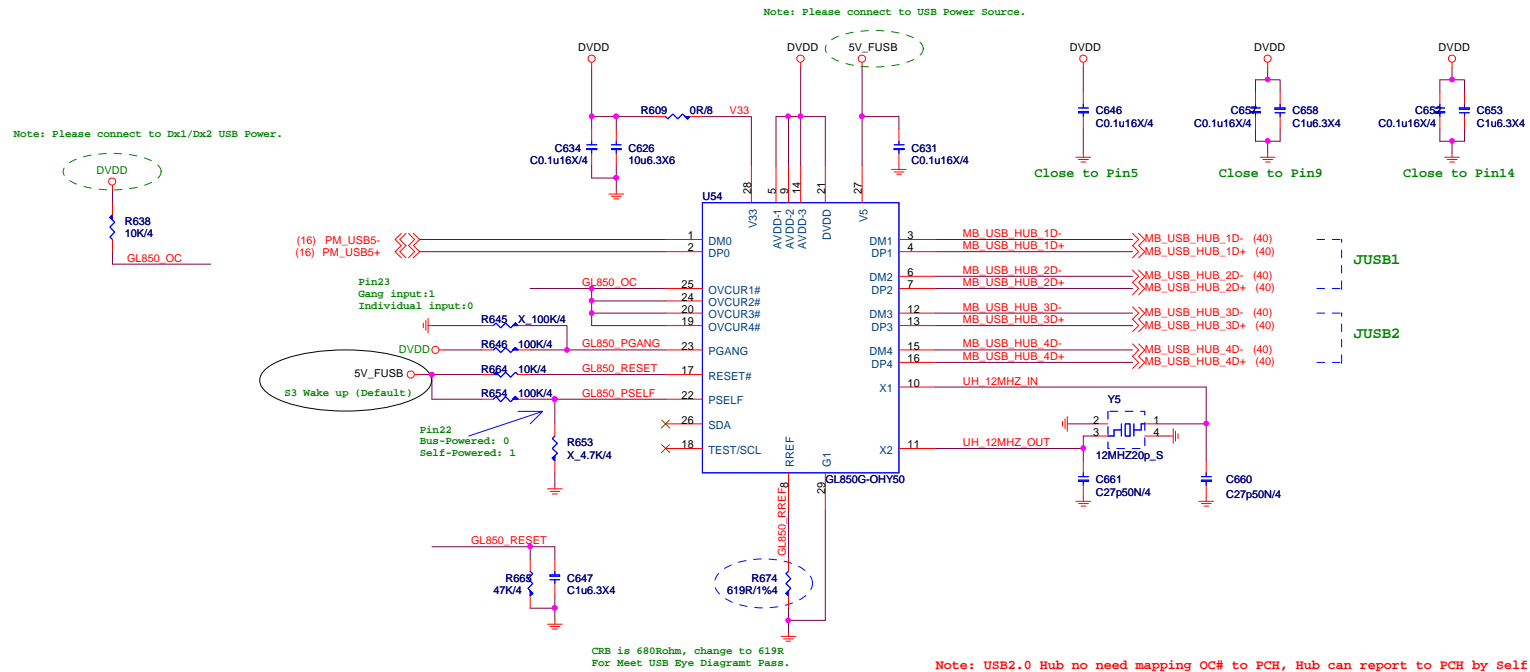
Current Mode



MICRO-STAR INT'L CO.,LTD			
MS-7C37			
Size Custom	Document Description		Rev 3.
	Blue USB3.1 Type C / MUX		
Date: Monday, May 06, 2019	Sheet	45	of 75

GL850G USB2.0 HUB

5V_FUSB



Note: USB2.0 Hub no need mapping OC# to PCH, Hub can report to PCH by Self.



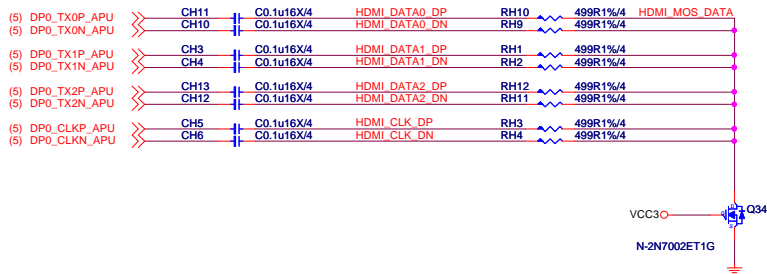
MICRO-STAR INT'L CO.,LTD

MS-7C37

Size Custom	Document Description GL850G	Rev 3.1
Date: Monday, May 06, 2019		Sheet 46 of 75

HDMI CONNECTOR

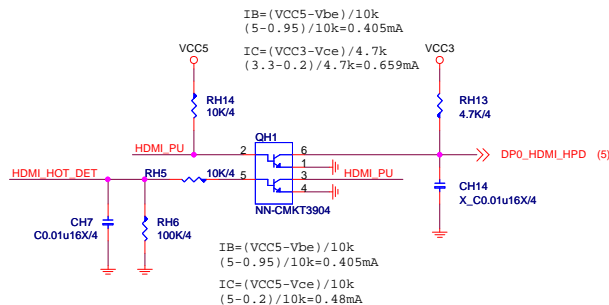
For HDMI 1.4



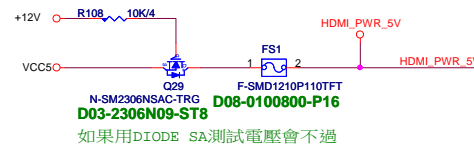
刪除RH6/RH12/RH15/RH16
For 增加VCC5寬度

For EMI

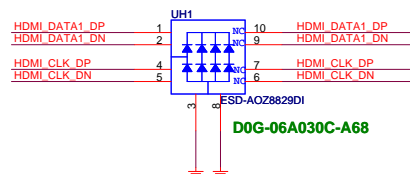
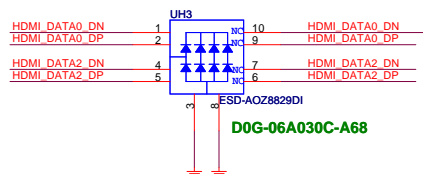
HPD Circuit



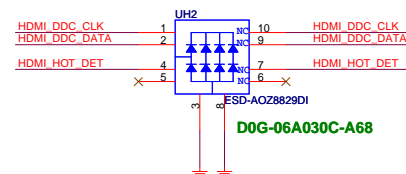
Connector Power



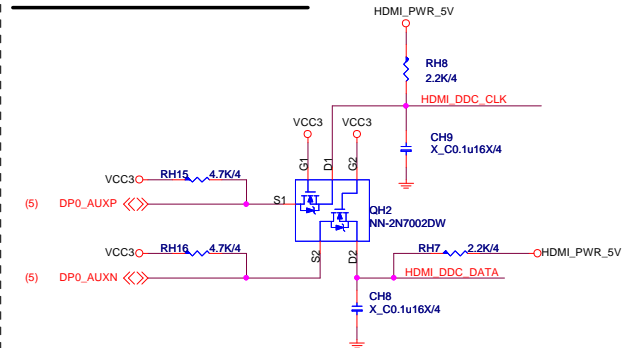
For EMI



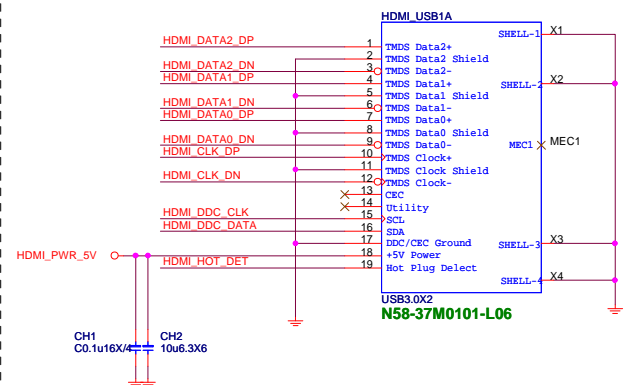
注意:耐壓5v零件



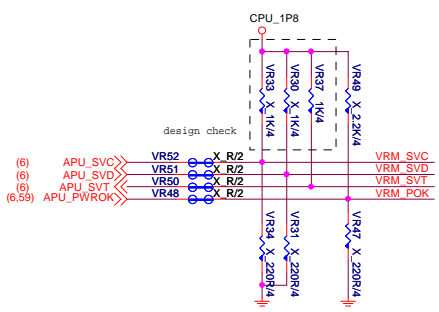
AUX Level Shifter



Connector

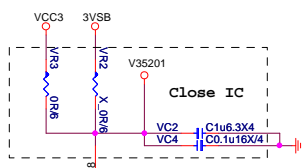
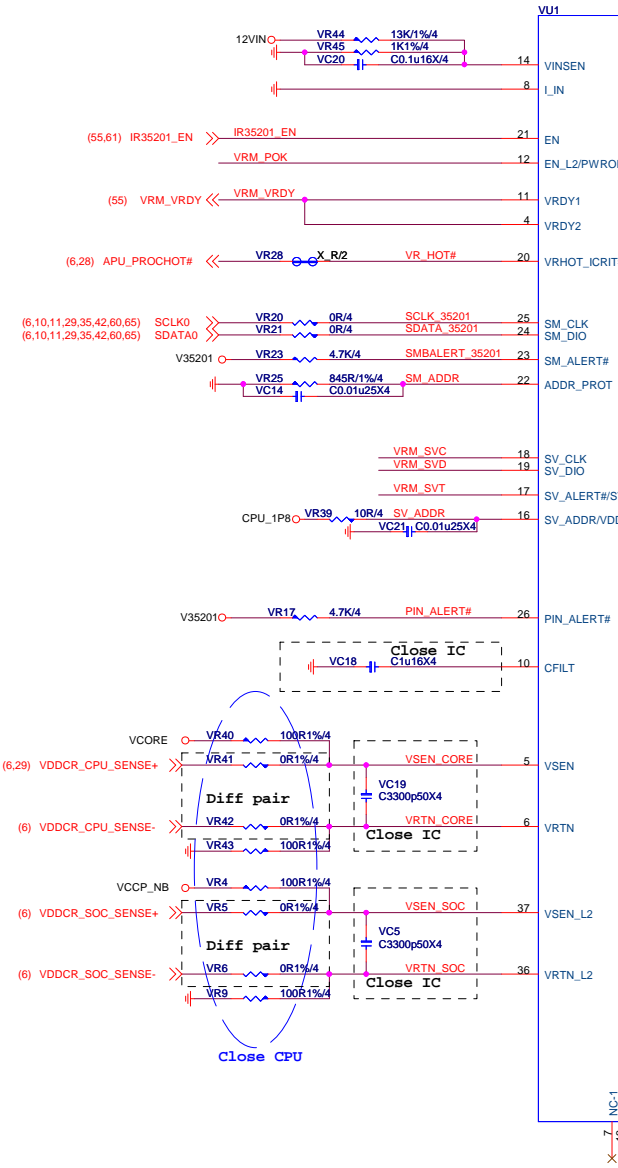
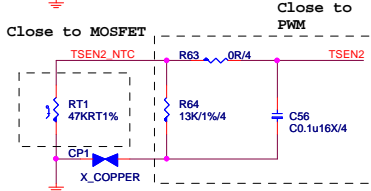
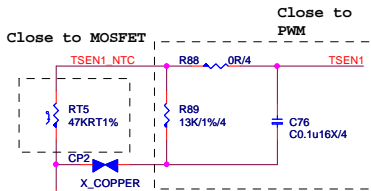
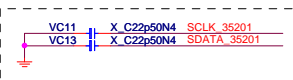
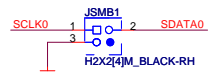
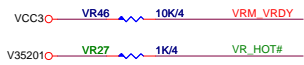


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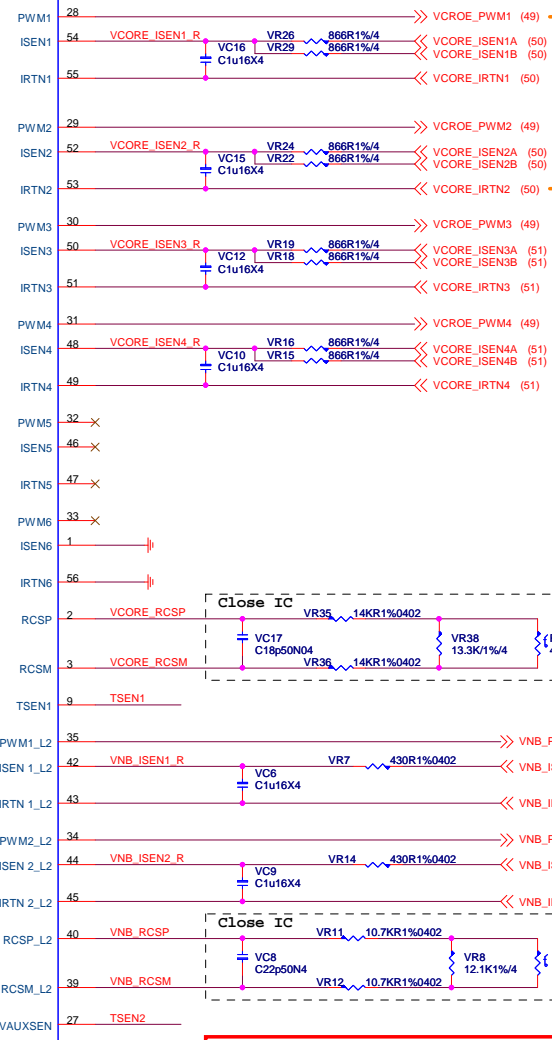


Note:VID Override Circuit

BOOT VOLTAGE		Pre_PWROK Metal VID
SVC	SVD	
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



燒錄打點:IC正面上橋+金色點



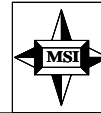
VCORE: ICCMax 140A
LL: 1.3mohm
OCP: 192A
SOC: ICCMax 75A
LL: 2.1ohm
OCP: 90A

Phase 1 close to CPU power pin.

RT close to Choke

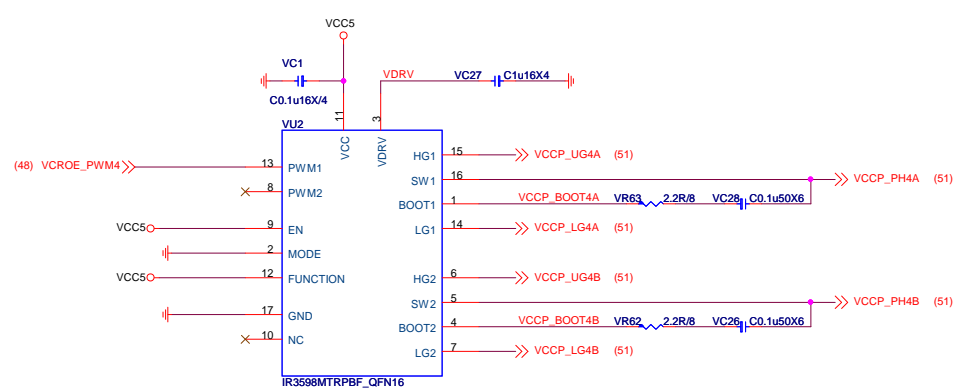
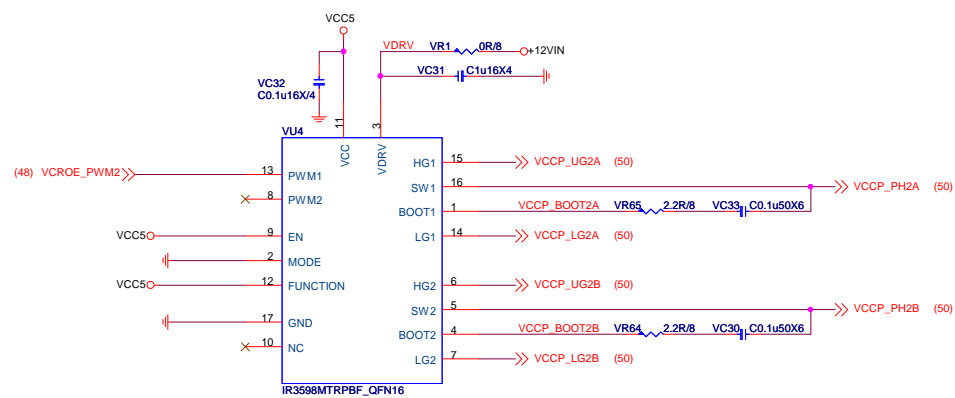
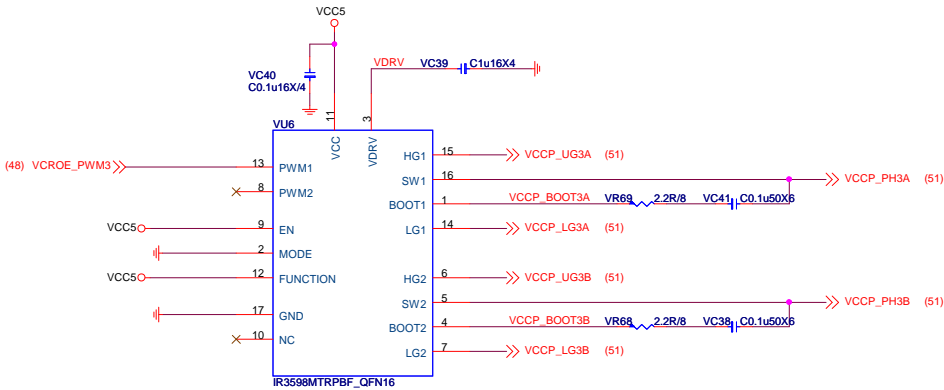
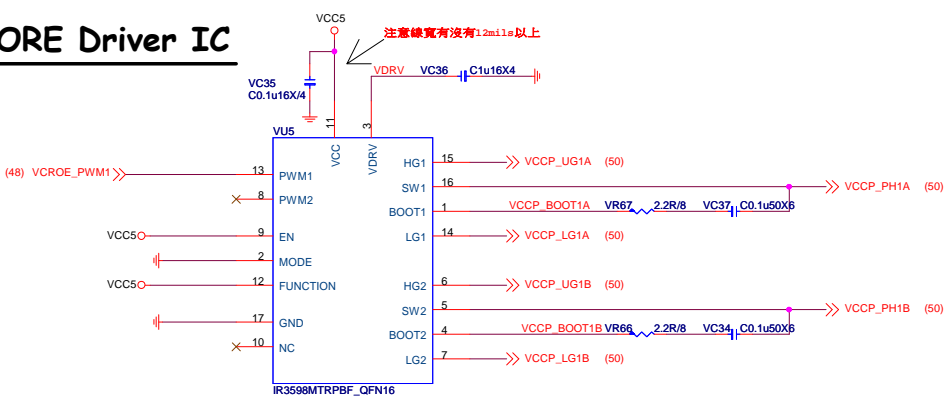
RT close to Choke

0x26:RH=18K,RL=13K							
Default	VR53	VR54	VC20	VR58	VR57	VR59	VR60
Temp	6.49k	10k	100p	X	0R	X	0R
VAUXSEN	5.76k	1k	0.01u	0R	X	0R	X



MICRO-STAR INT'L CO.,LTD			
MS-7C37			
Size Custom	Document Description		Rev 3.1
		CPU Power IR35201 8+2	
Date: Monday, May 06, 2019		Sheet 48	of 75

CPU_CORE Driver IC



CPU_SOC Driver IC

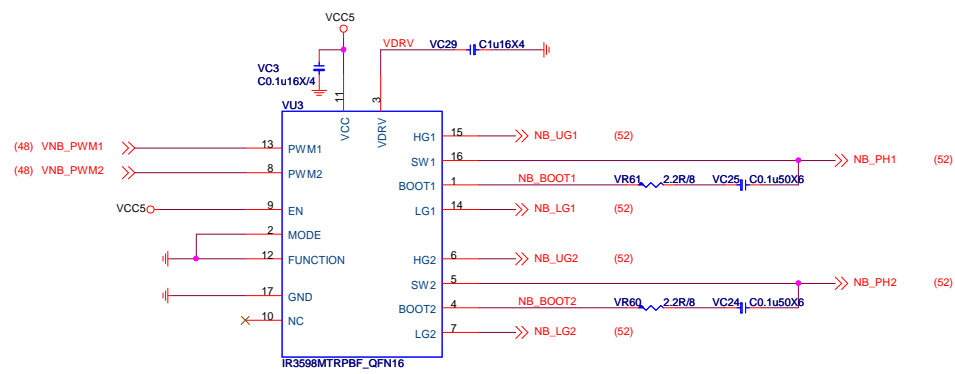


Table for IR3598				
Function	Mode	PWM Mode	Phase Mode	
0	1	IR ATL	Dual	
1	1	IR ATL	Doubler	
0	0	Tri-State	Dual	SOC
1	0	Tri-State	Doubler	Vcore

MICRO-STAR INT'L CO.,LTD

MS-7C37

CPU Power Driver IC IR3598

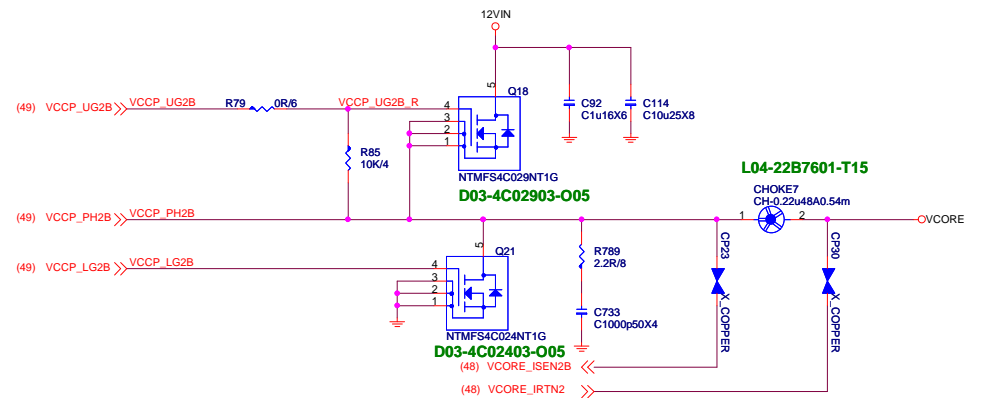
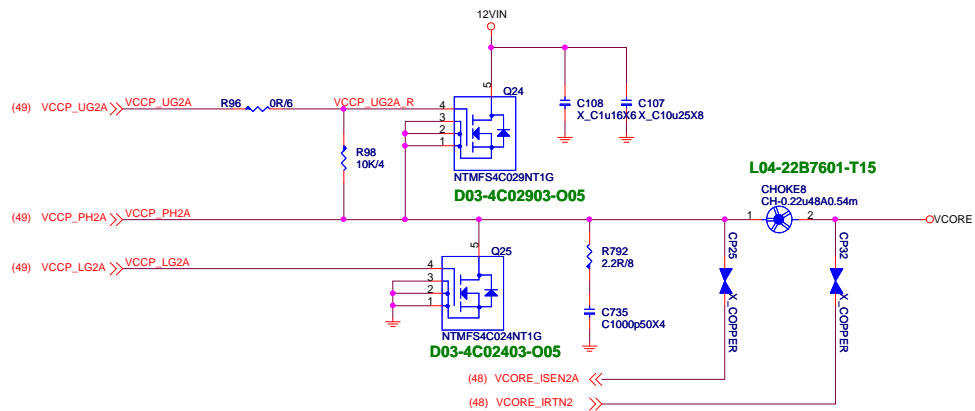
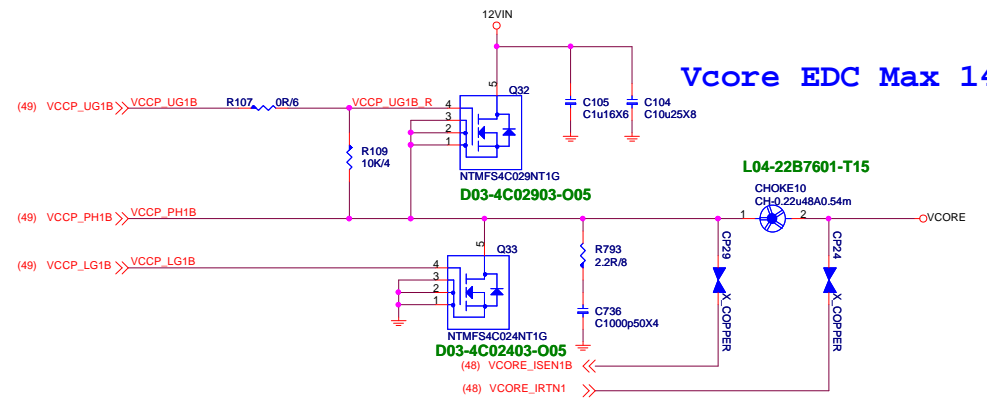
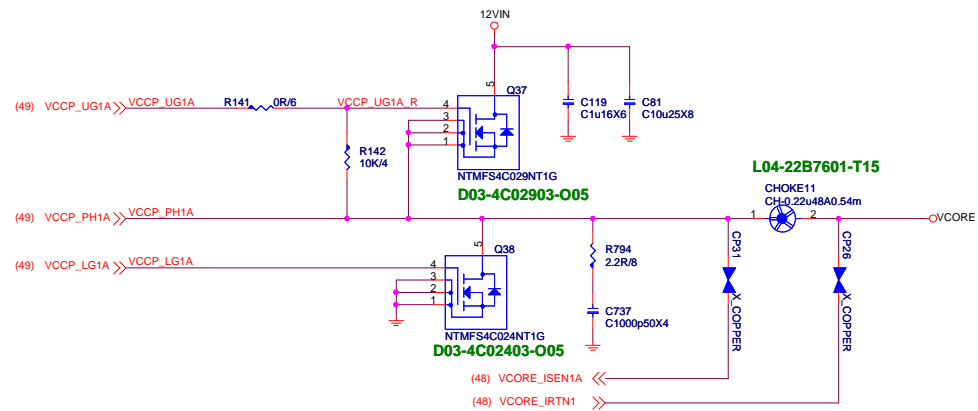
Size Custom

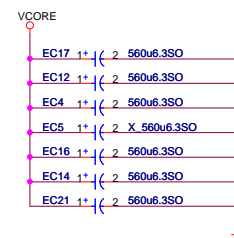
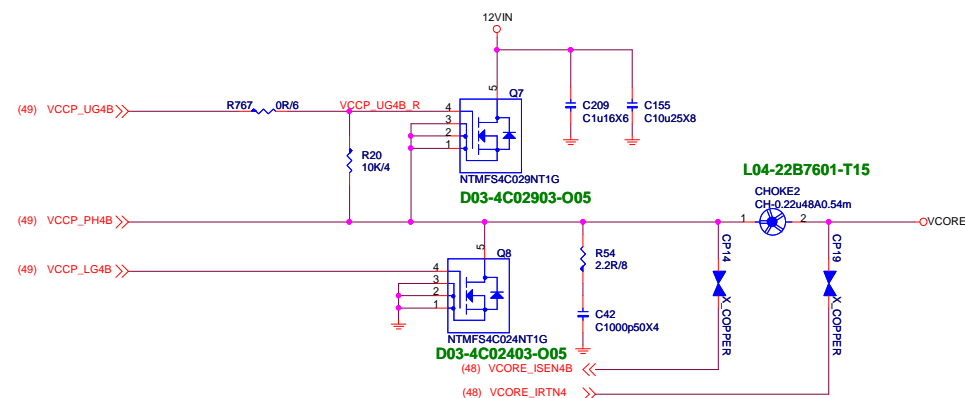
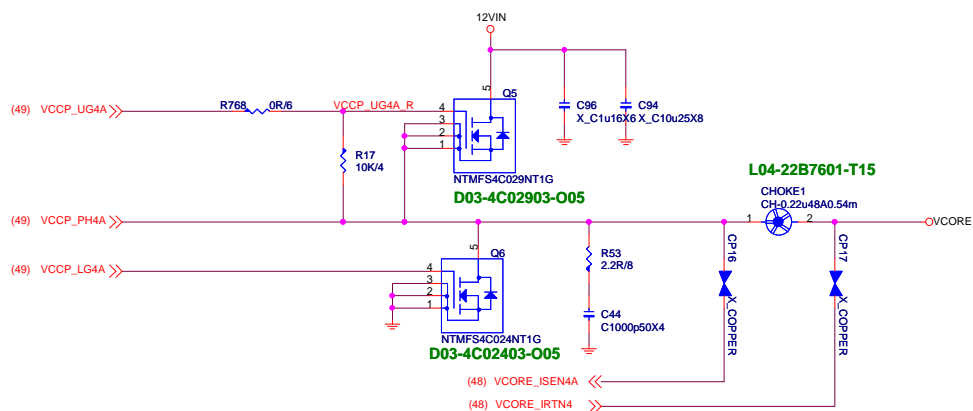
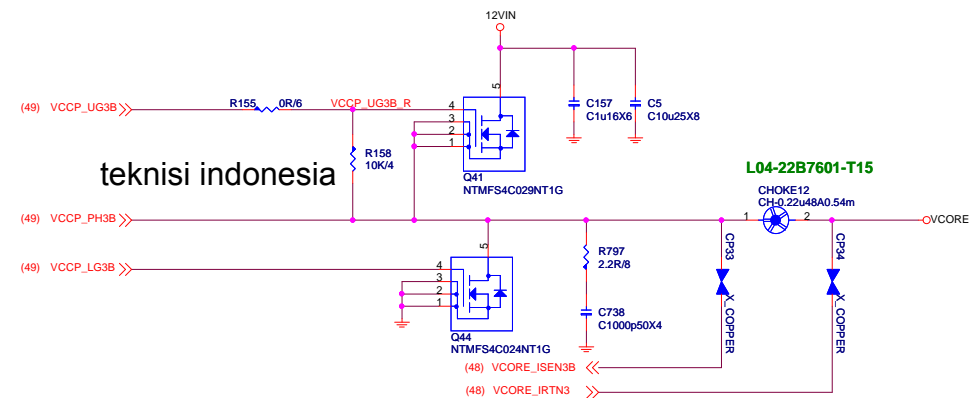
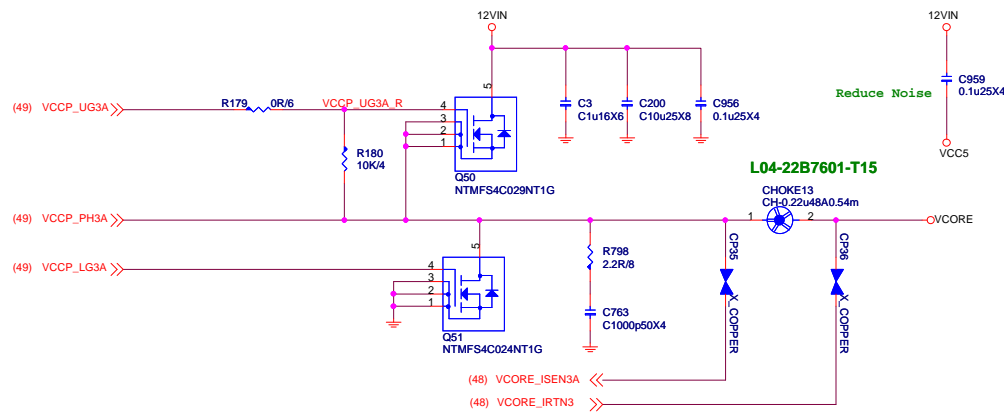
Document Description

Date: Monday, May 06, 2019

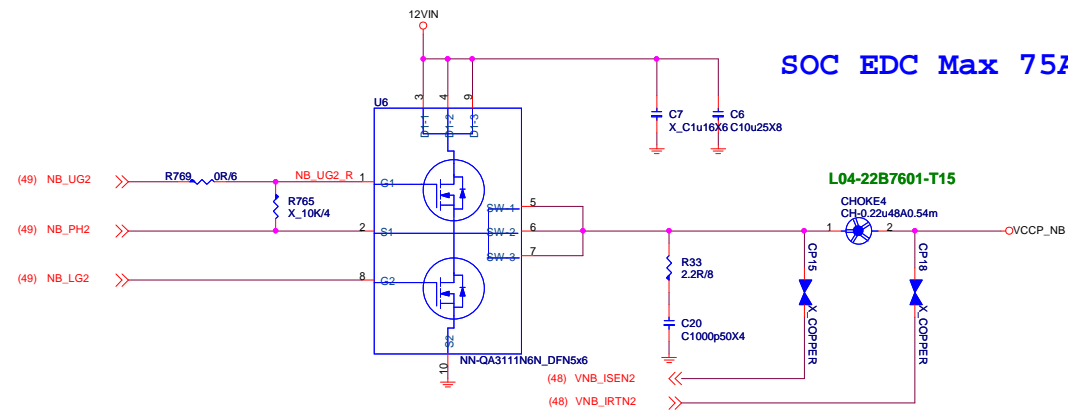
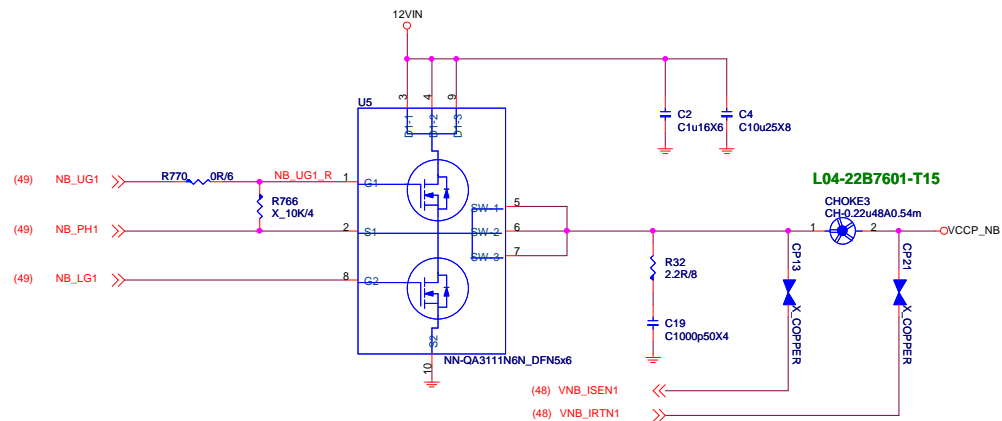
Rev 3.1

Sheet 49 of 75

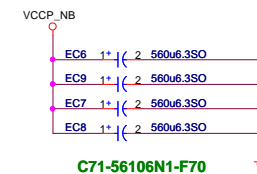




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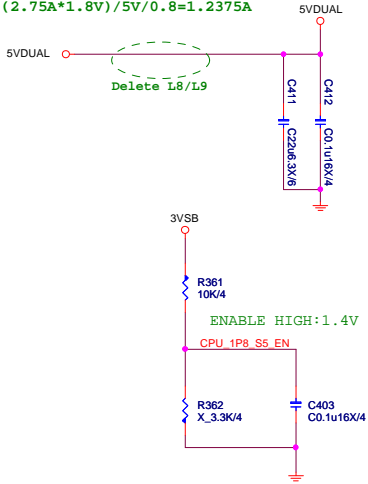
SOC EDC Max 75A



```
CPU: VDD_18_S5@0.5A
CPU: VDDIO_Audio@0.25A
CHIP: VDD_18_S5@0.1A
```

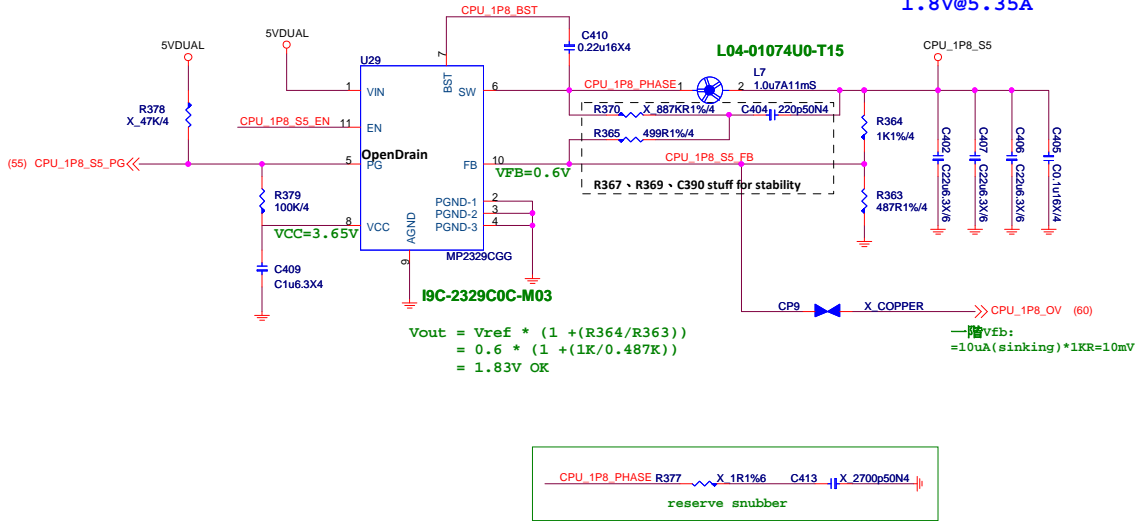
```
CPU_1P8: 2.5A
CPU_VDDP_S5: 1A
CHIP_SOC_S5: 1A
```

Input Current=
 $(2.75\text{A} \times 1.8\text{V}) / 5\text{V} / 0.8 = 1.2375\text{A}$

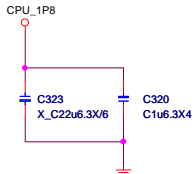
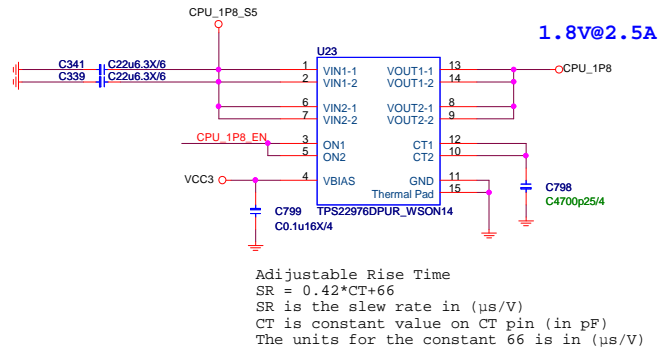
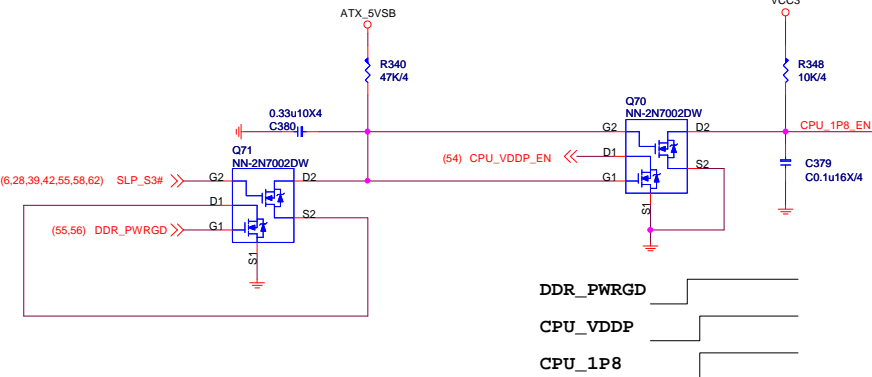


CPU_1P8_BST、CPU_1P8_BST_R >50 mils.

1.8V@5.35A



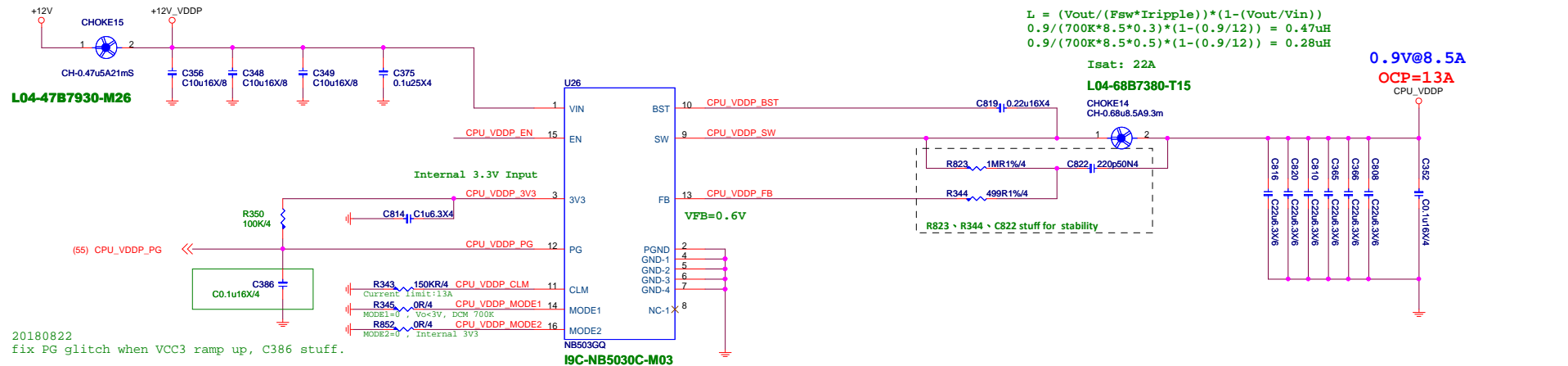
CPU: VDD_18@2A
CHIP: VDD_18@0.5A



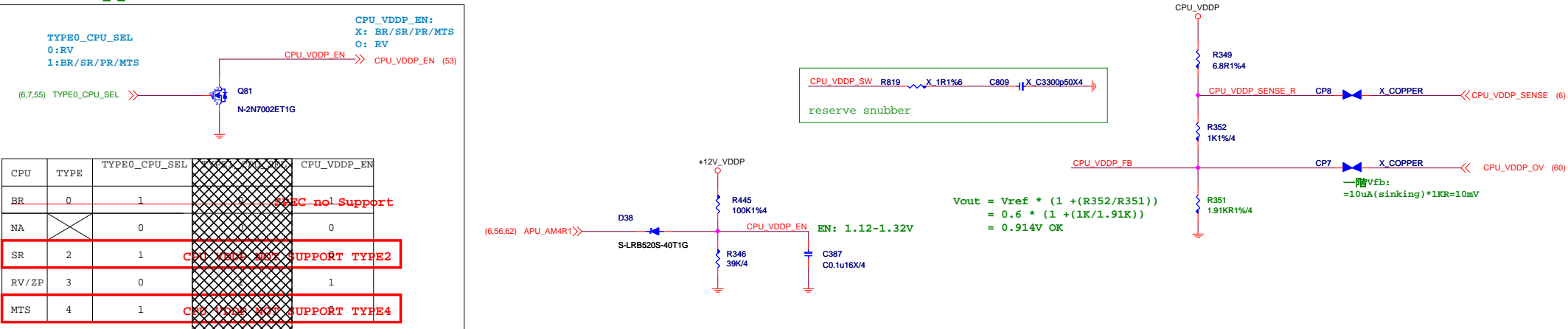
MICRO-STAR INT'L CO.,LTD			
MS-7C37			
Size Custom	Document Description CPU Power 1.8_S0 / S5		Rev 3.1
Date: Monday, May 06, 2019		Sheet 53 of	75

CPU: VDDP@8.5A

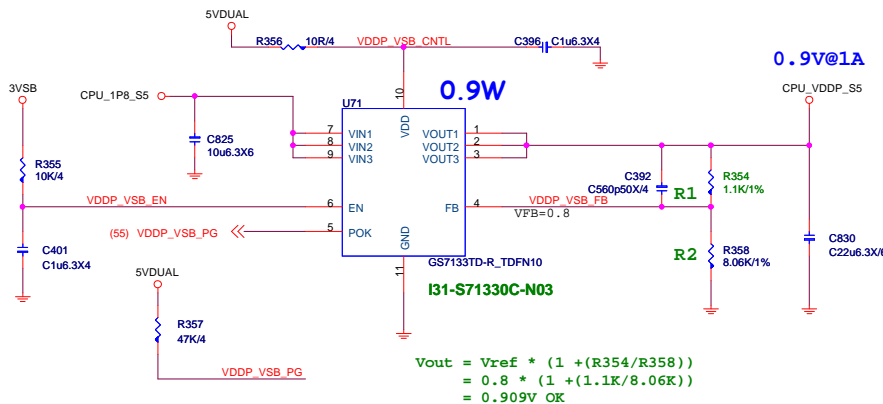
```
Input Current = (8.5A*0.9V)/12V/0.8 = 0.8A
Choke Isat = 8A
Irms=Iout*SQRT((Vo/Vi)*(1-(Vo/Vi)))
=13*SQRT((0.9/12)*(1-(0.9/12))) = 3.42A
Choke Irms =5 A
```



No support BR SPEC



CPU: VDDP_S5@1A



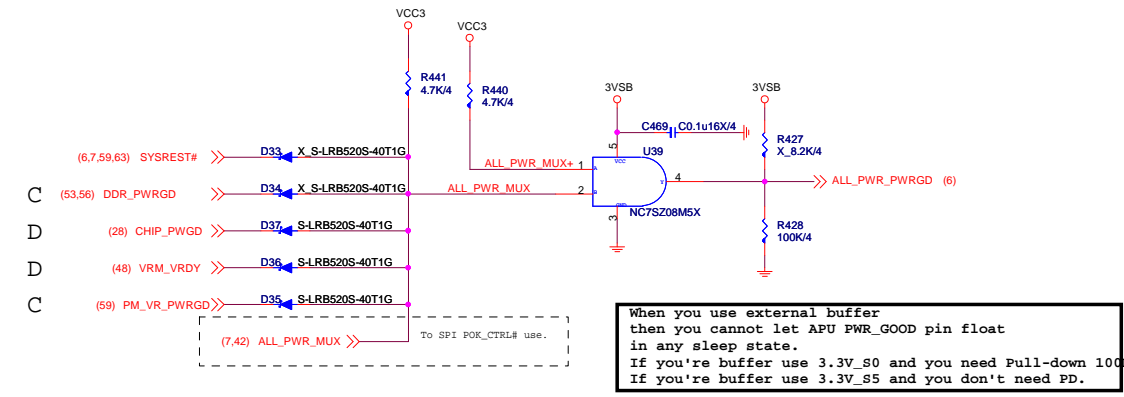
MICRO-STAR INT'L CO.,LTD

MS-7C37

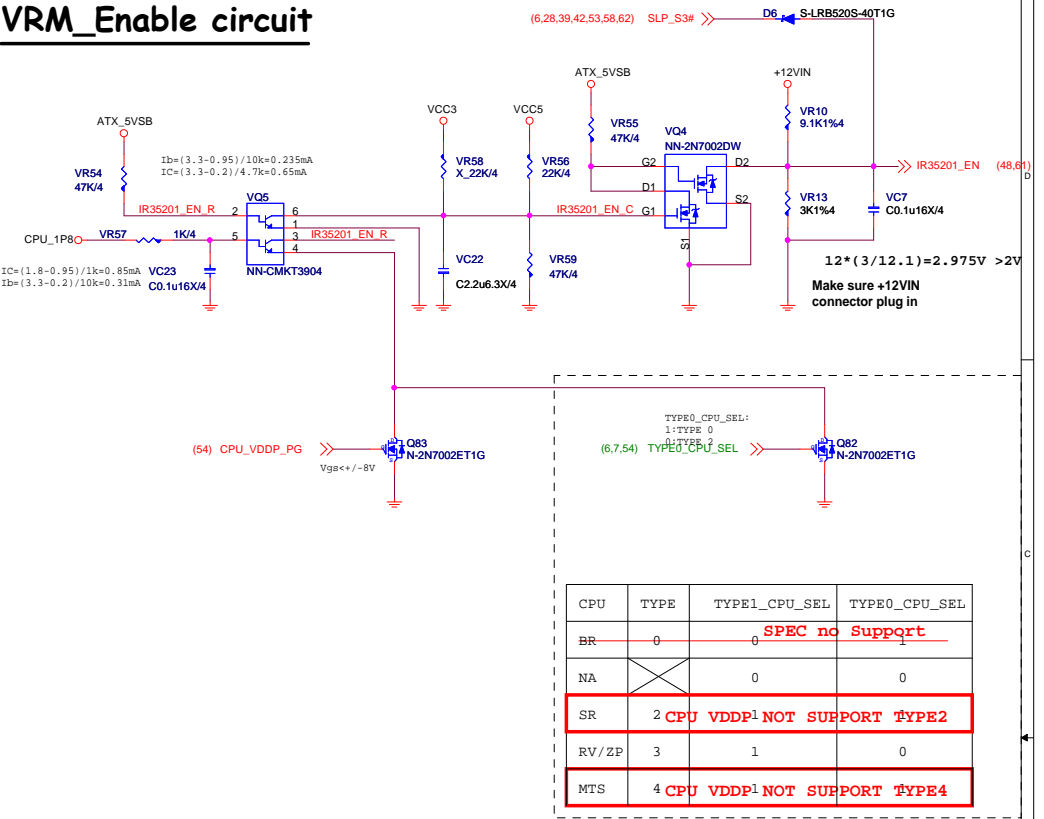
Size Custom	Document Description CPU Power VDDP - NB503	Rev 3.1
Date: Monday, May 06, 2019		Sheet 54 of 75

ALL POWER GOOD MUX

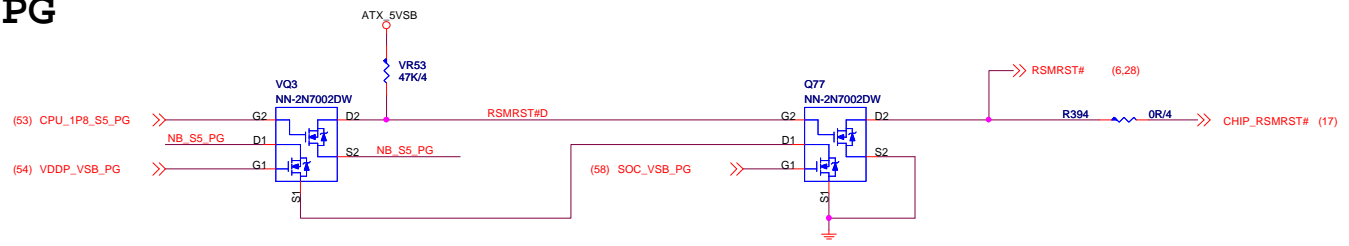
S0 PG



VRM_Enable circuit



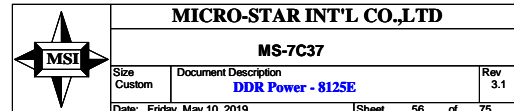
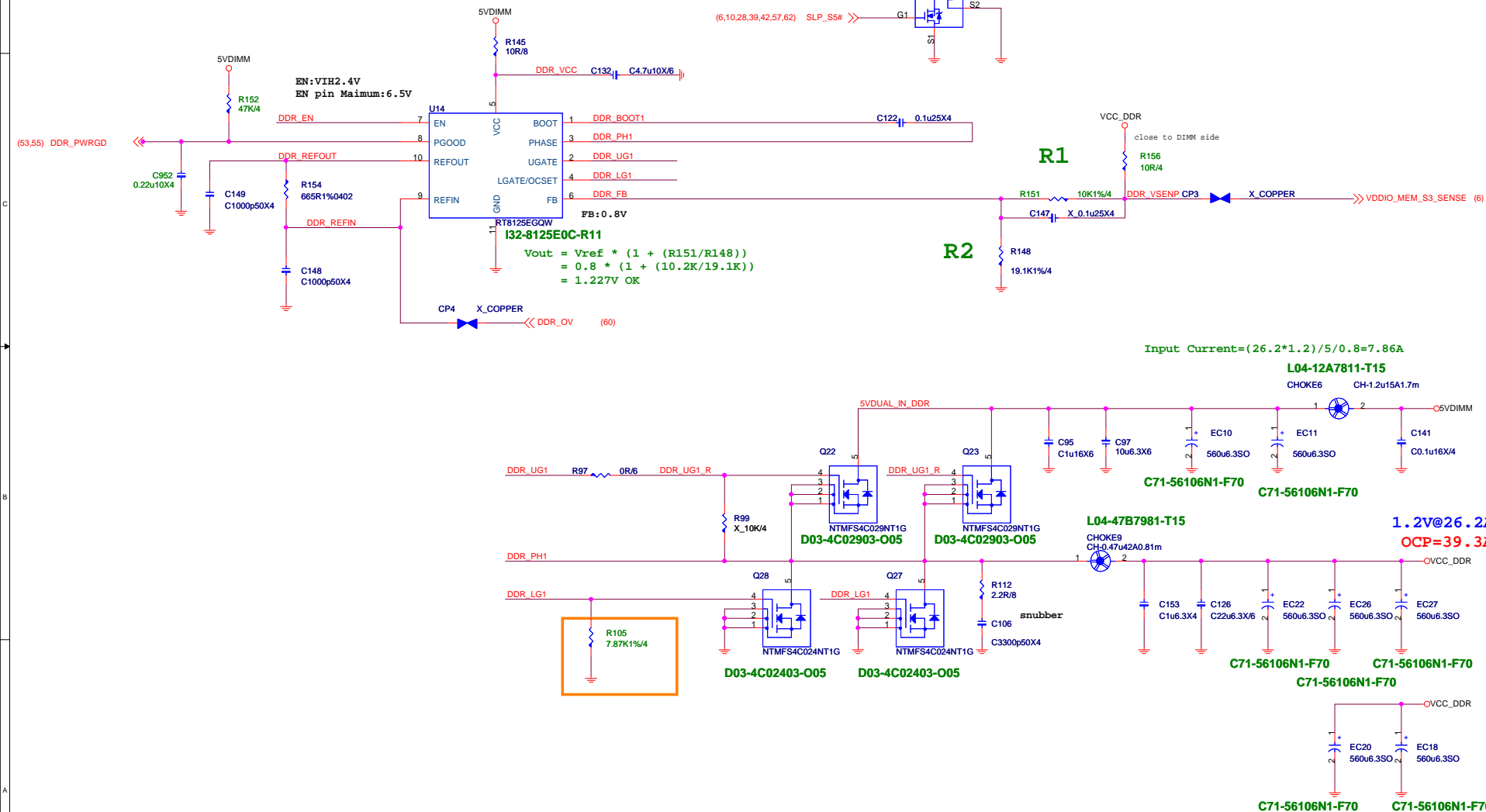
S5 PG



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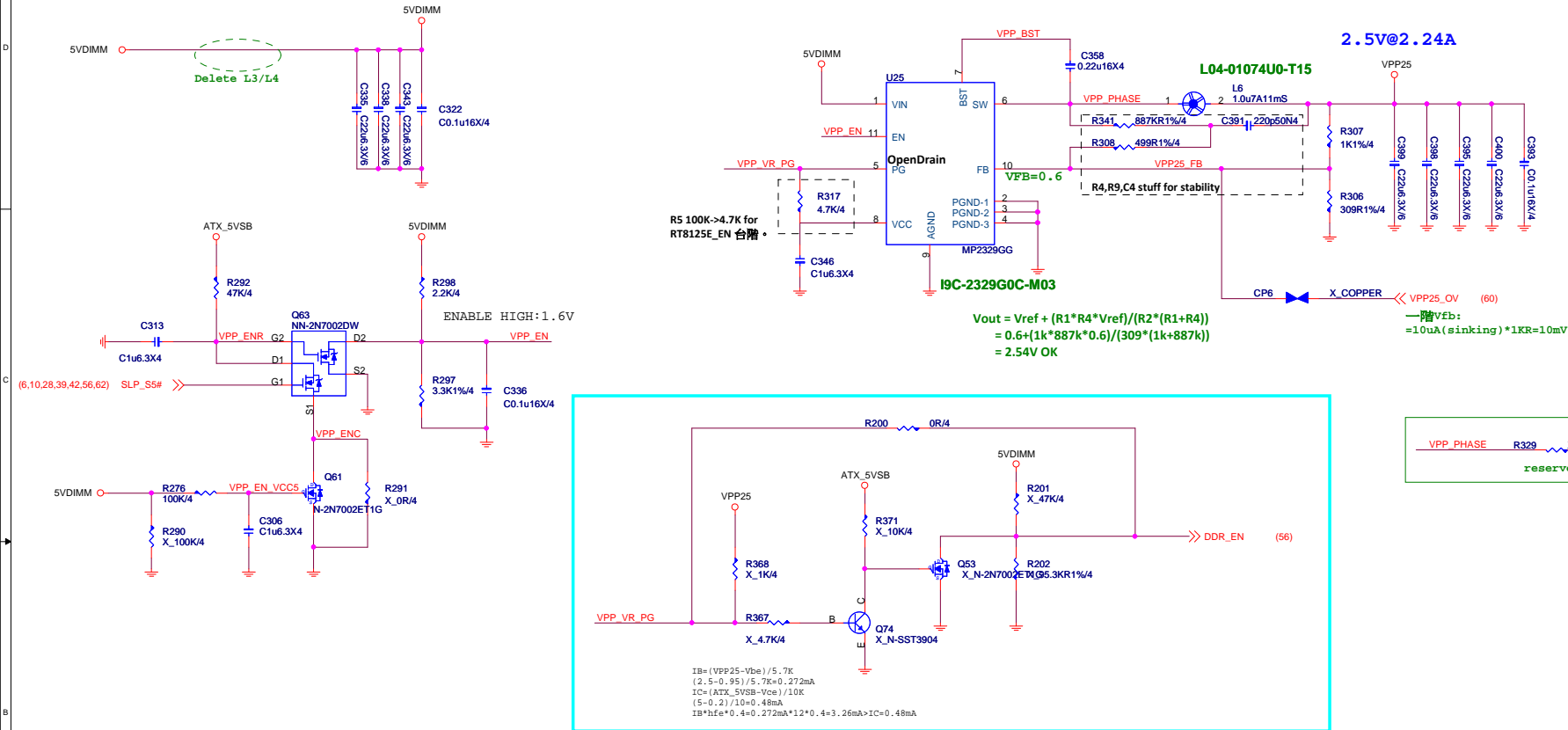
15.5A For CPU
9.5A For 4DIMM
1.2A For DDR VTT

Current Sensing				
losses			9	10
				11
				μA



VPP25

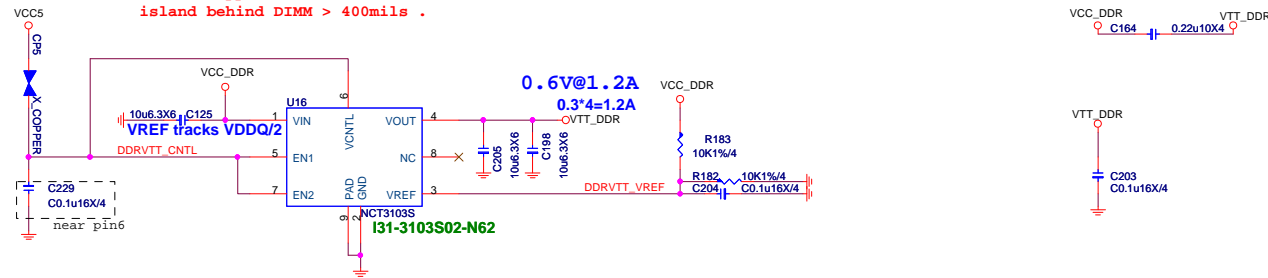
2.5V@2.24A



VTT_DDR

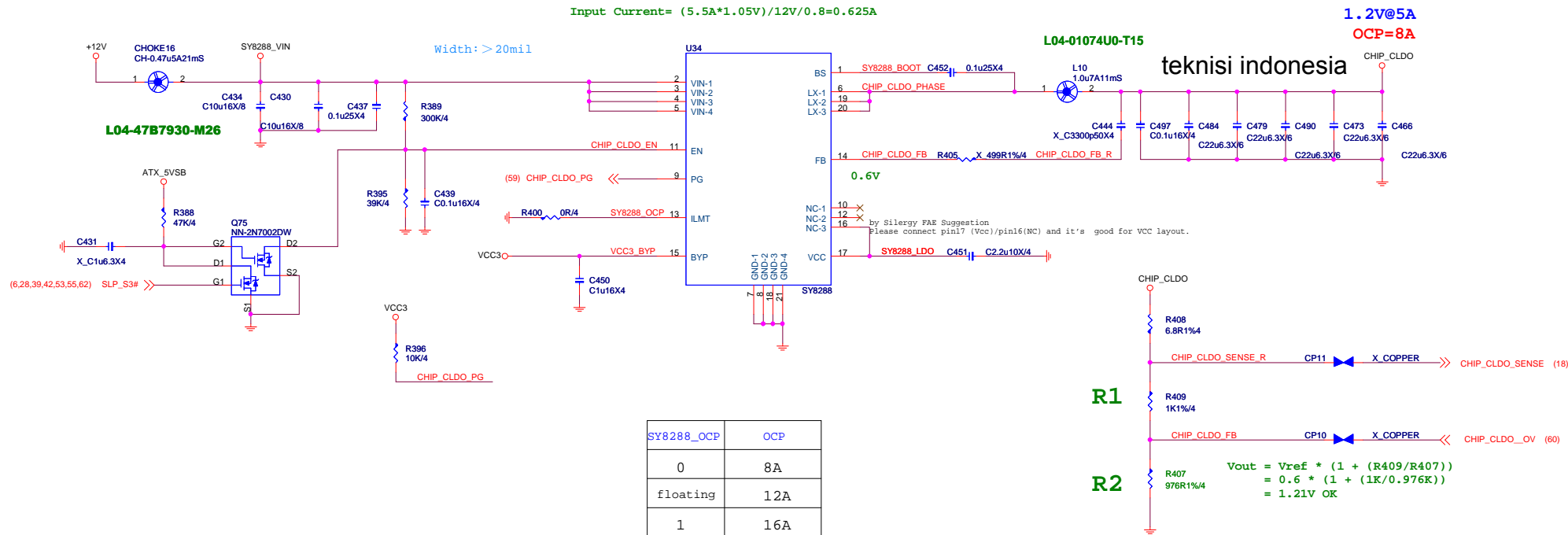
0.6V@1.2A

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



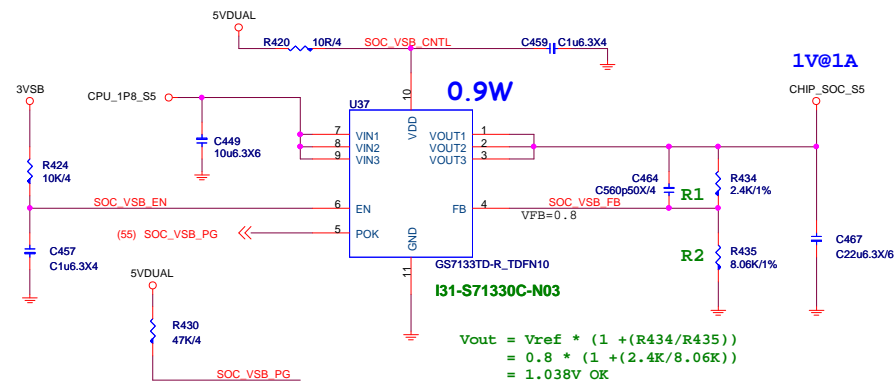
CHIP_CLDO

CHIP: VDD_CLDO@5A



CHIP_SOC_S5

CHIP: VDDCR_SOC_S5@1A



CHIP_SOC

CHIP: VDDCR_SOC@9A

Input Current = $(12A \cdot 1V) / 12V / 0.8 = 1.25A$
 Choke Isat = 8A
 $I_{rms} = I_{out} \cdot \sqrt{((V_o/V_i) \cdot (1 - (V_o/V_i)))}$
 $= 12 \cdot \sqrt{((1/12) \cdot (1 - (1/12)))} = 3.316A$
 Choke Irms = 5 A

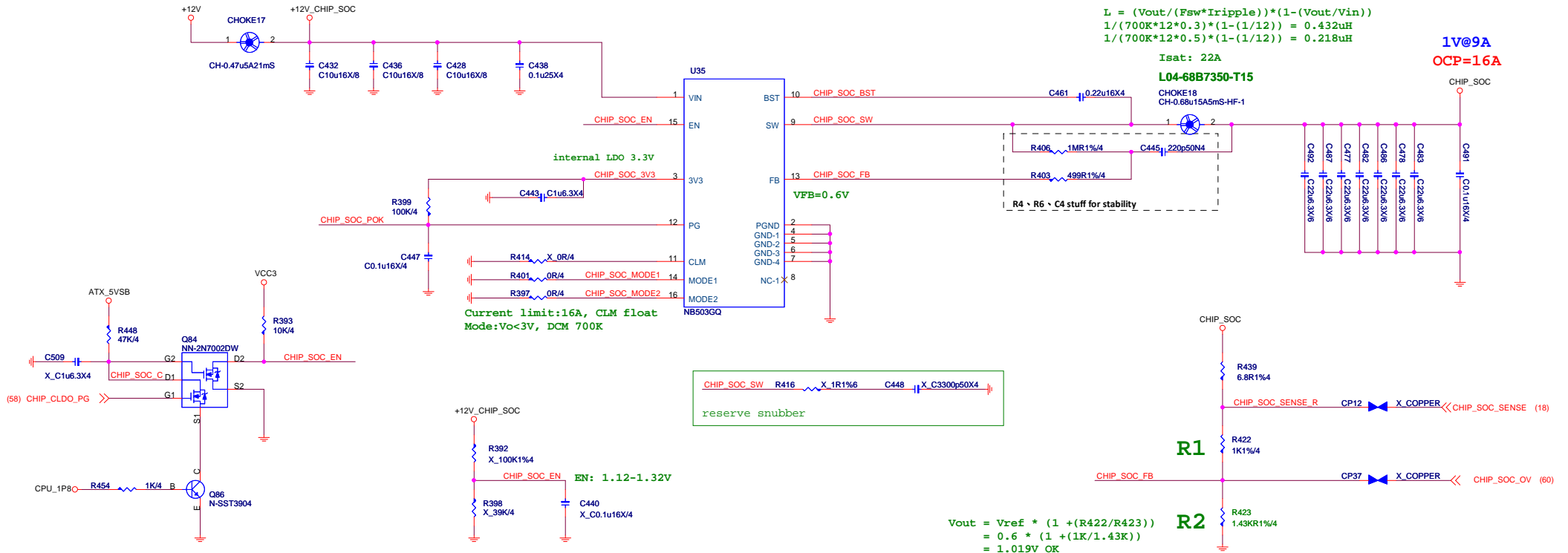
$L = (V_{out} / (F_{sw} \cdot \Delta I_{ripple})) \cdot (1 - (V_{out}/V_{in}))$
 $1 / ((700K \cdot 12 \cdot 0.3) \cdot (1 - (1/12))) = 0.432uH$
 $1 / ((700K \cdot 12 \cdot 0.5) \cdot (1 - (1/12))) = 0.218uH$

Isat: 22A

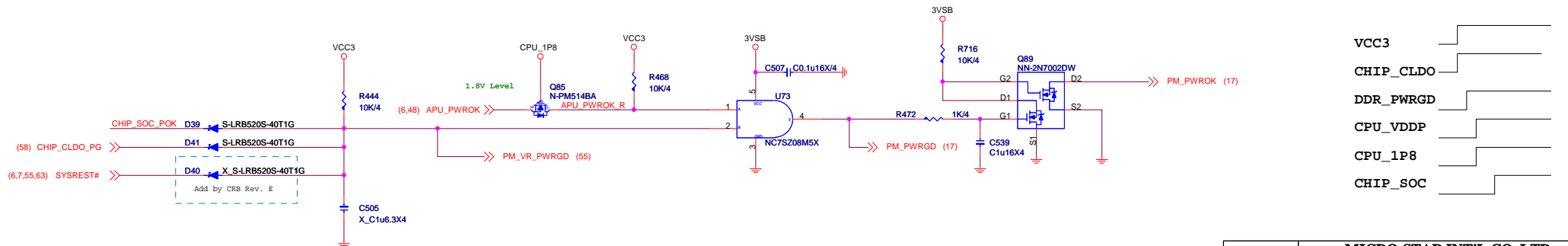
L04-68B7350-T15

CH-0.68u15A5ms-HF-1

1V@9A
 OCP=16A



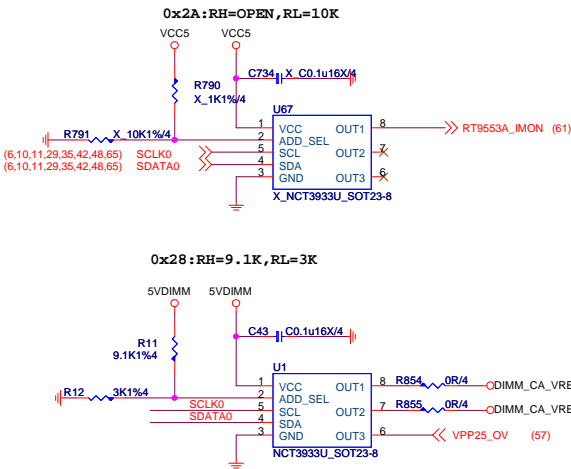
S0 PG



VCC3	
CHIP_CLDO	
DDR_PWRGD	
CPU_VDDP	
CPU_1P8	
CHIP_SOC	

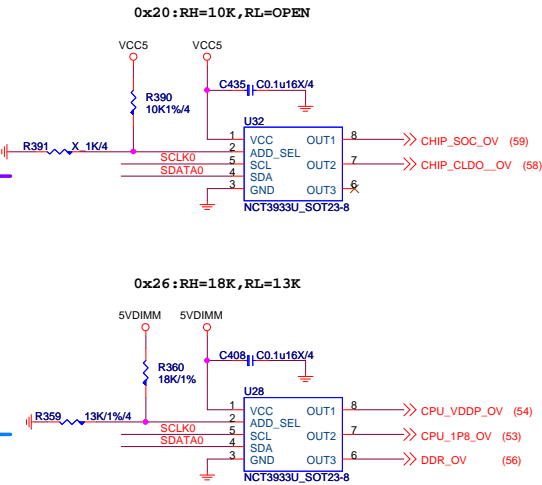
MICRO-STAR INT'L CO.,LTD			
MS-7C37			
Size	Document Description	Rev	
Custom	PROM - NB503 / 1.0V	3.1	
Date:	Monday, May 06, 2019	Sheet	59 of 75

Over Voltage Control IC



UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

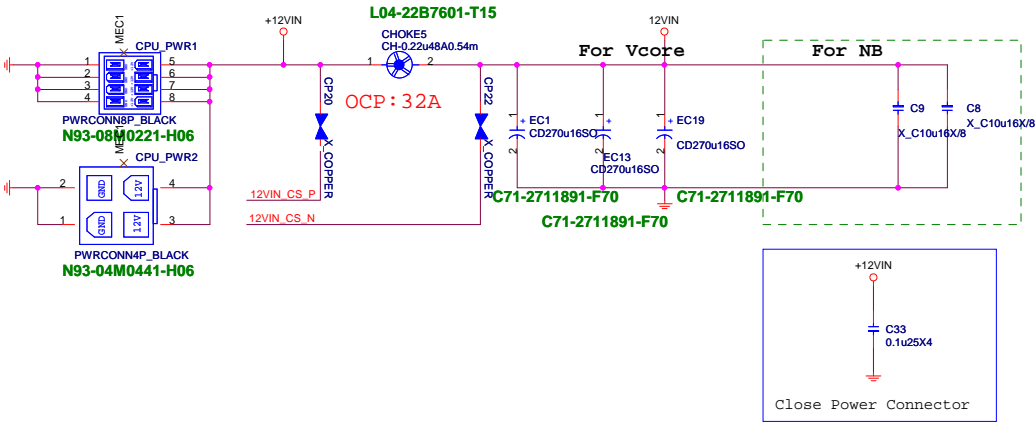


UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

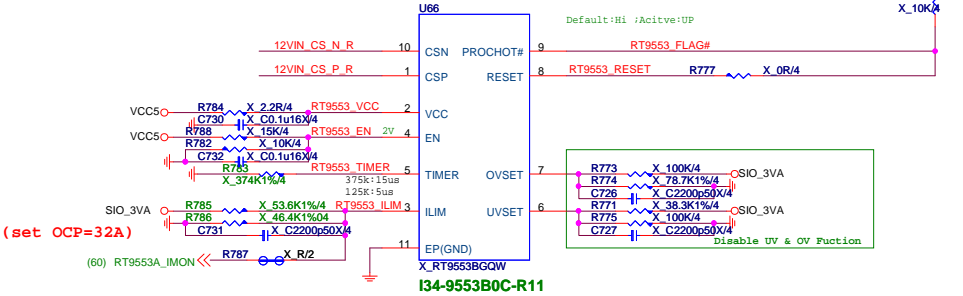


CPU POWER CONNECTOR

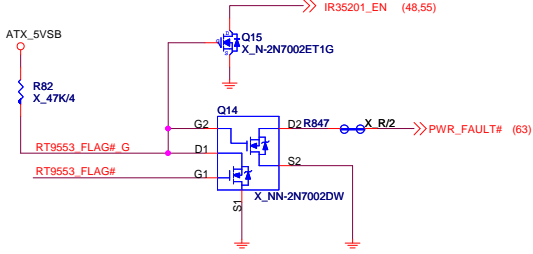
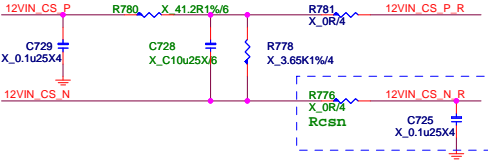


RT9553B CURRENT SENSE

RT9553 PIN5: When start OV/UV, RESET delay time can meet SPEC 15us.

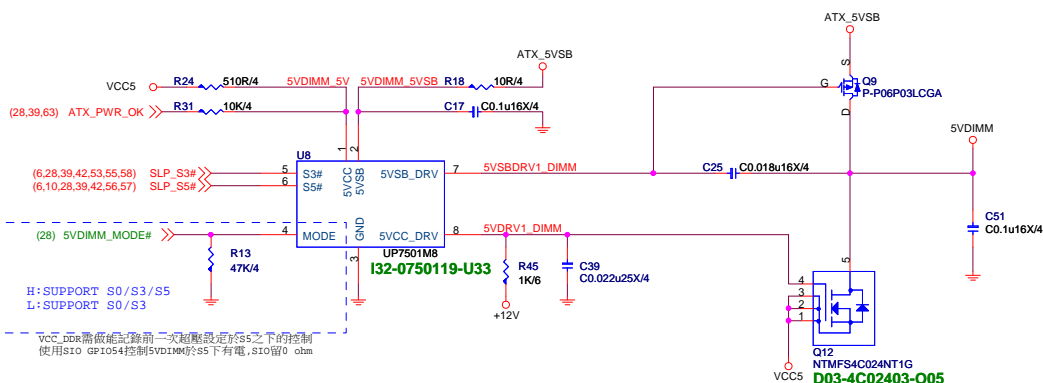


Vcore		SOC	
D=Vout/Vin		D=Vout/Vin	
Vin = 12	> input voltage	Vin = 12	> input voltage
Vout = 2	> output Vcore	Vout = 1.55	> output Vcore
D = 0.166667		D = 0.129167	
Io = Icore(max)*0.8		Io = Icore(max)*0.8	
I core(max) = 200	> Vcore current	I core(max) = 75	> Vcore current
I avg. = 160	A	I avg. = 60	A
I ripple={ Io*√ D*√ (1-D) } / Phase		I ripple={ Io*√ D*√ (1-D) } / Phase	
Phase = 10	phase	Phase = 2	phase
I ripple = 5.962848	A	I ripple = 10.06153	A
How many pcs. Of Cap.		How many pcs. Of Cap.	
I ripple(cap) = 4700	m A	I ripple(cap) = 4700	m A
COETEMP = 1		COETEMP = 1	
Input Cap. = 2	pcs.	Input Cap. = 3	pcs.



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5VDIMM FOR DDR



3VSB cost down

3.3V@3.363A

CPU: VDD_33_S5@0.25A

CHIP: VDD_33_S5@0.1A

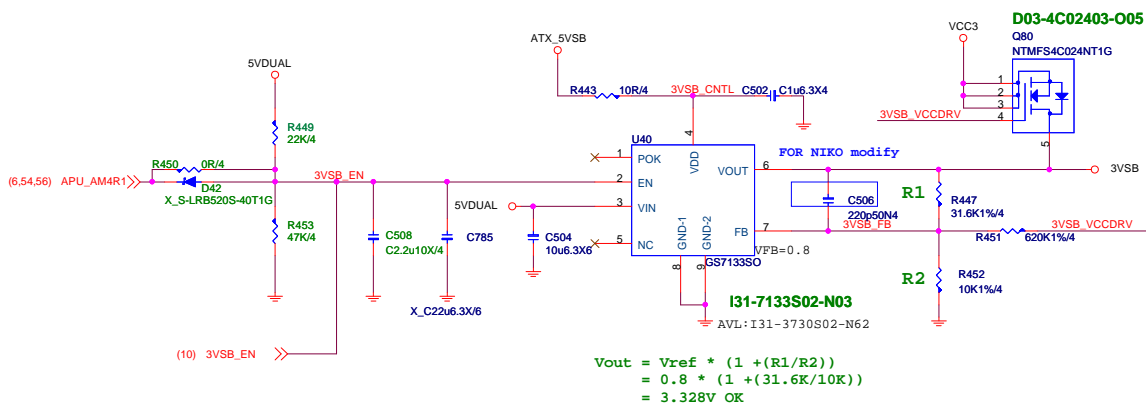
PCIE*4@1.5A

M.2_WIFI@0.78A

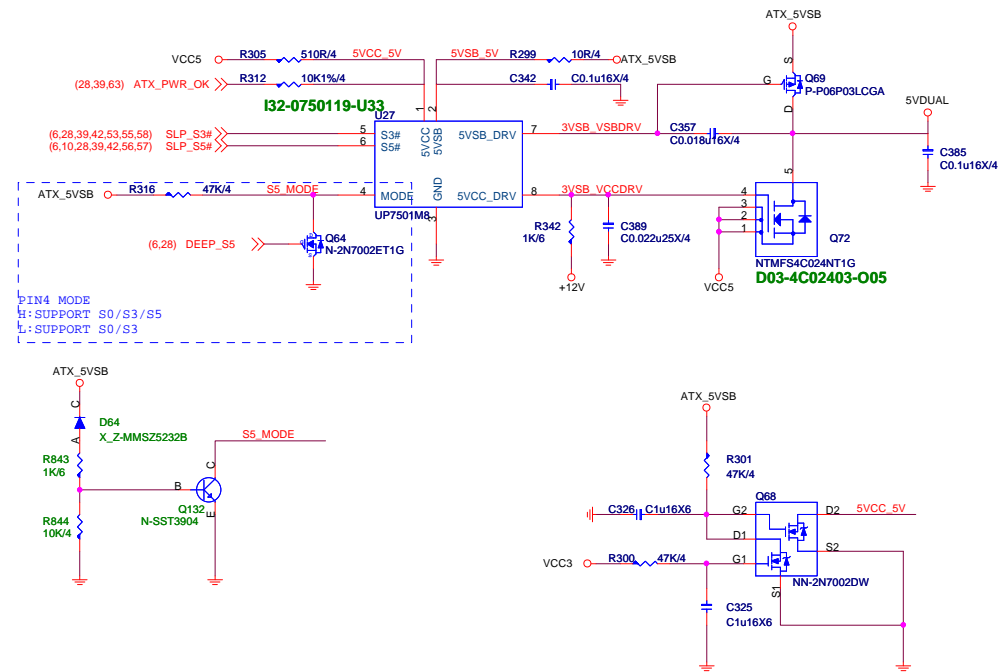
LAN@0.065A

Redriver*2@0.668A

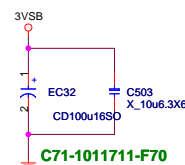
USB TYPE-C@0.9mA



5VDUAL For 3VSB、CPU 1.8V、 VDDP



```
| For power 700W solution (only for uP7501+uP7506 for 3VSB solution)|
| The power supply VCC3 delay 12ms after VCC5 assert.              |
| The chip U7501 5VDRV1 work when the VCC5 ready                  |
| (When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but    |
| VCC3 not ready and let the 3VSB sequence fail.                  |
```



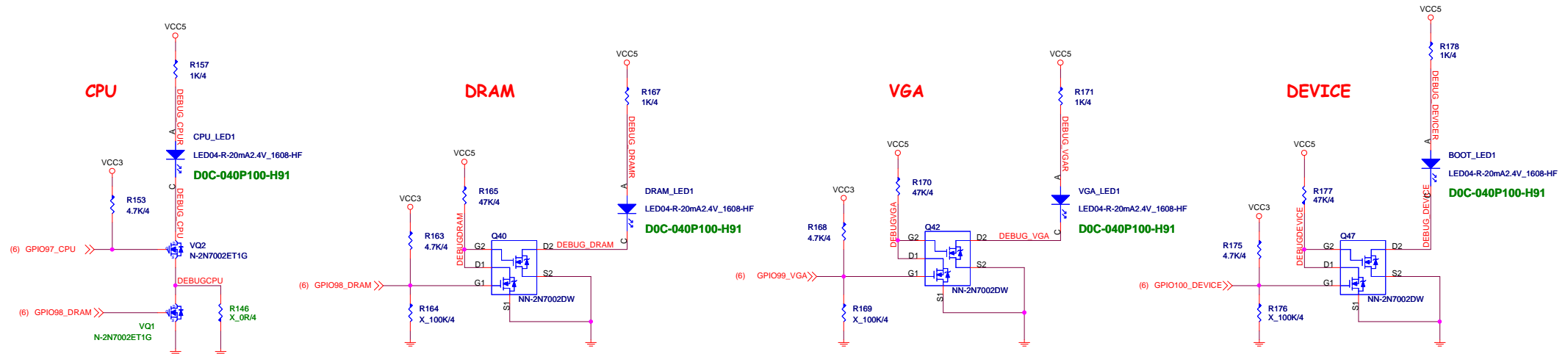
MICRO-STAR INT'L CO.,LTD

MS-7C37

Size Custom	Document Description ACPI - 3VSB / 5VDIMM	Rev 3.1
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Date: Monday, May 06, 2019	Sheet 62 of 75
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EZ Debug LED



LED亮燈時同時將CPU LED關掉

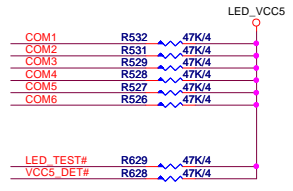
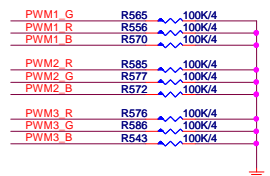
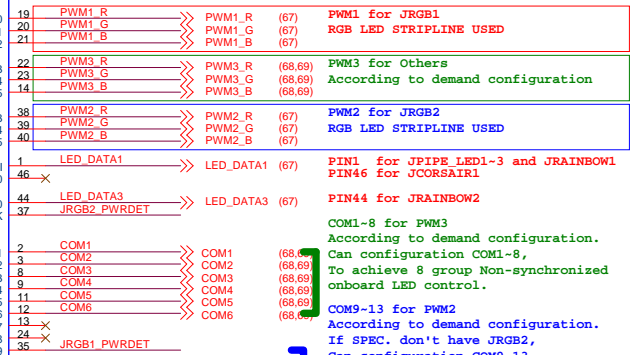
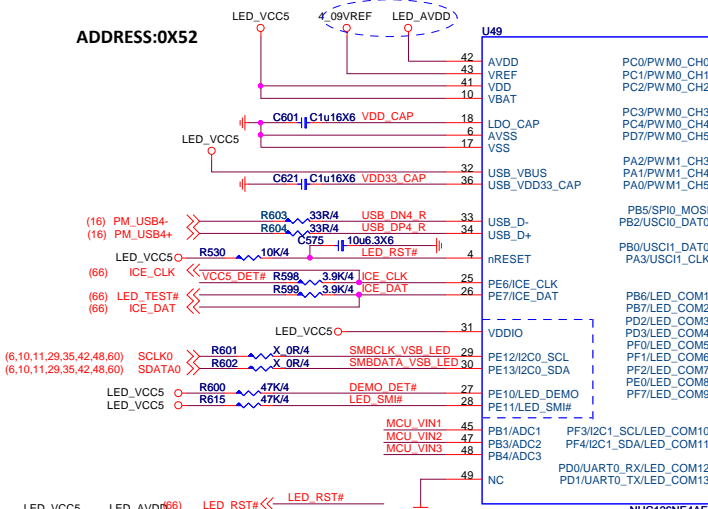
LEDGPIO	GPIO97	GPIO98	GPIO99	GPIO100
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

AMD AMP Detect LED

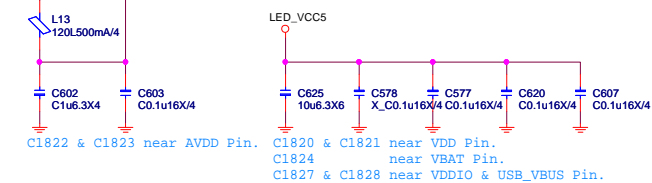
48 PIN LED MCU

If you use ADC function, need to separate VREF from AVDD and 4_09VREF stuff for VREF.

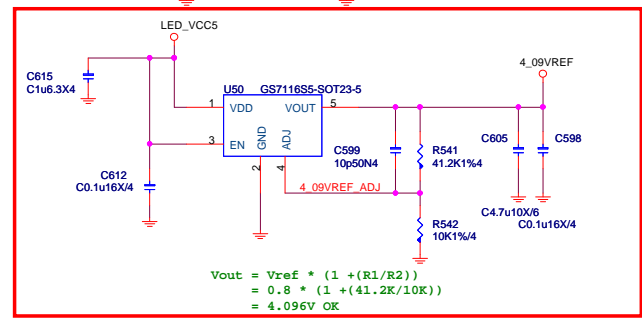
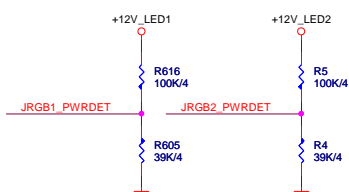
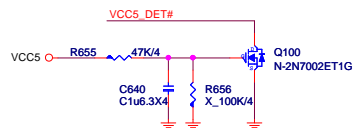
ADDRESS:0X52



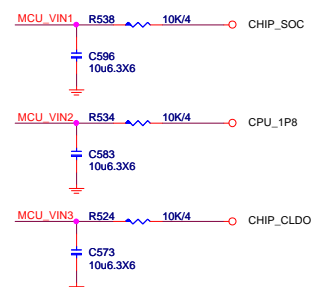
PS. COM1 is the first action block, next is COM2, and so on. Pin15,16 can configure to master smbus if spec requirement.



If SPEC has LED demo function without demo button, DEMO_DET# must pull up to LED_VCC5,Q319 need to stuff and control by LED_VCC5_EN. PS. R630 remove, R600 and Q101 need to stuff



Option Spec For Voltage Monitor Require.



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Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_GPIO_03	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1~8	PWM3
Board Side LED	COM 9~13	PWM2

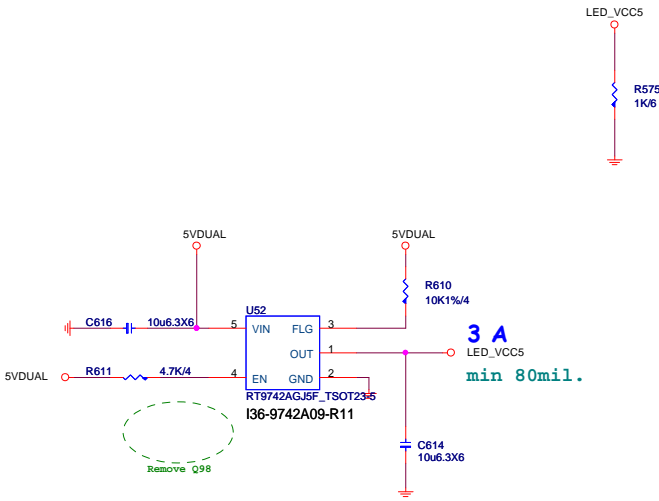
MICRO-STAR INT'L CO.,LTD

MS-7C37

Size Custom Document Description **MCU - LED Control** Rev 3.1

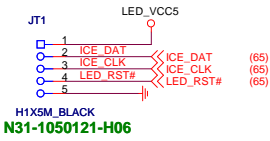
Date: Monday, May 06, 2019 Sheet 65 of 75

EXTERNAL POWER INPUT



External Power

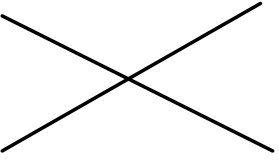
JT1 for FW update



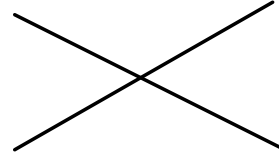
JF1 For Factory Test



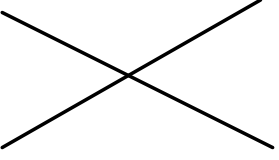
1 PCH HEATSINK LED



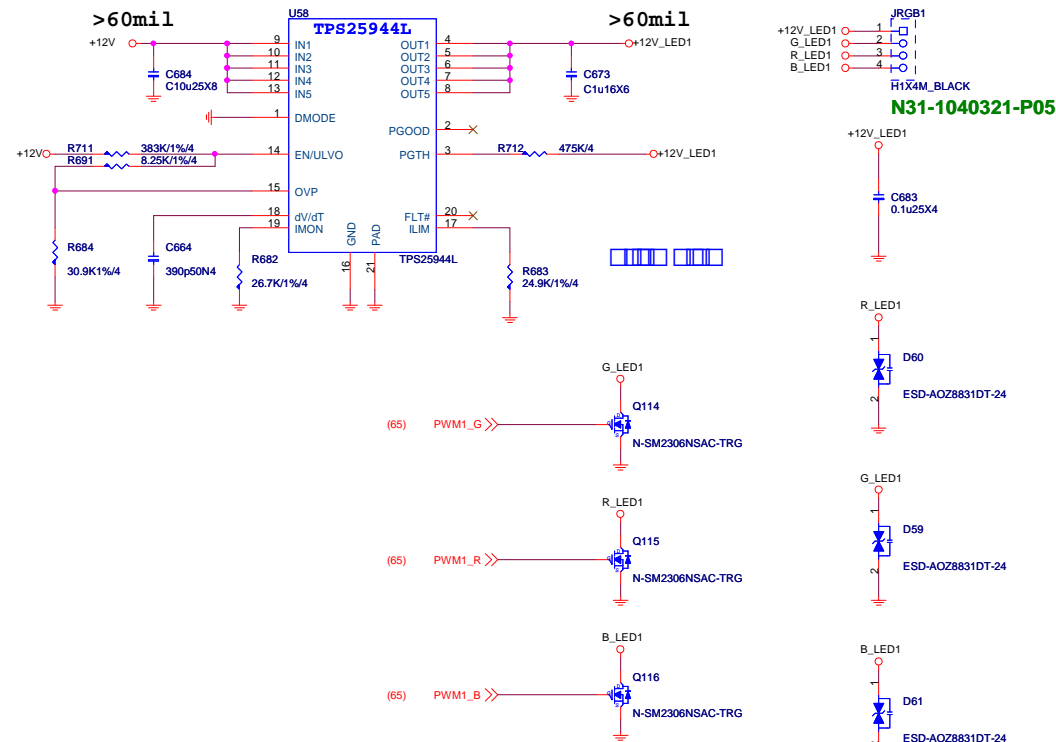
2 AUDIO/IO Cover LED



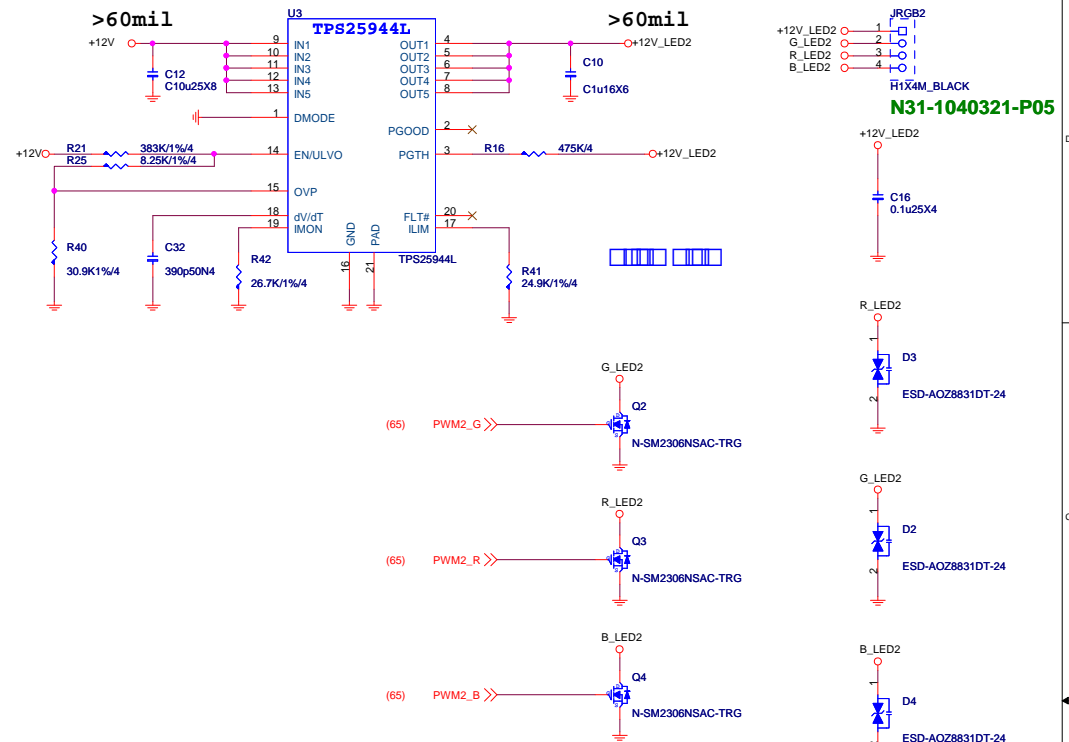
3 MOS HEATSINK LED



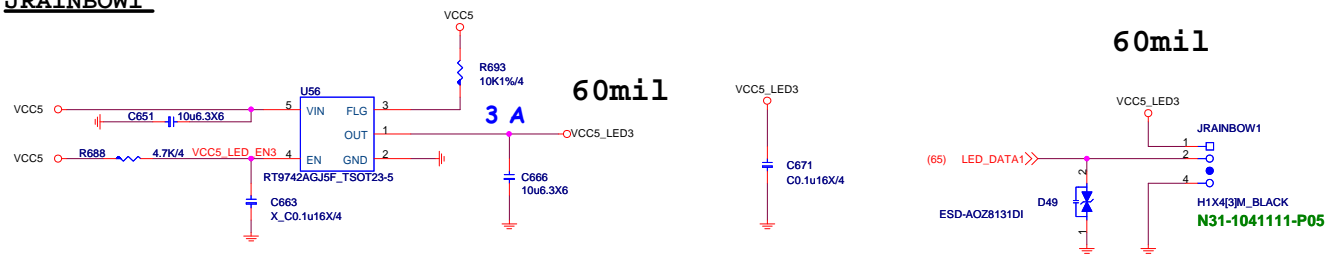
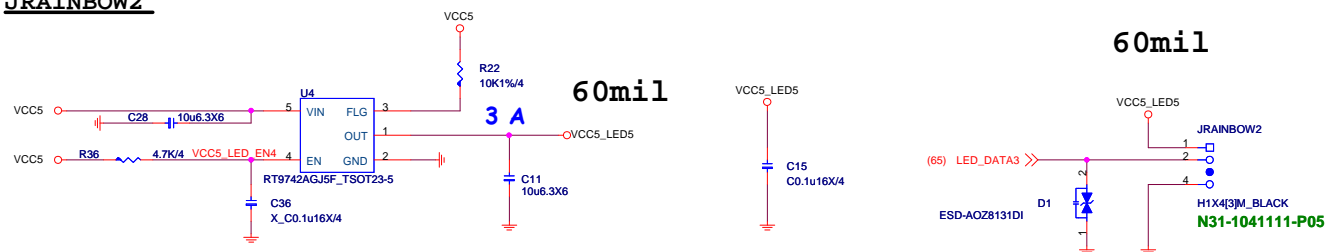
JPIPE:PIN1:output ,PIN2:input
PIN2:MCU IN
PIN1:HEATSINK OUT

JRGB1

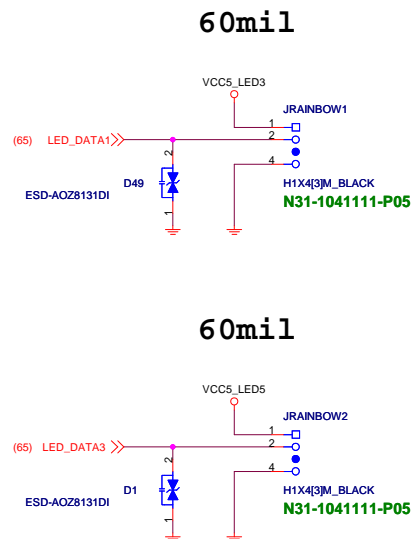
外接LED 燈條 (RGB)
 ---- PCB 文字面 (JRGB1)
 ---- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺

JRGB2

----- 外接LED 燈條 (RGB)
----- PCB 文字面 (JRGB2)
----- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺

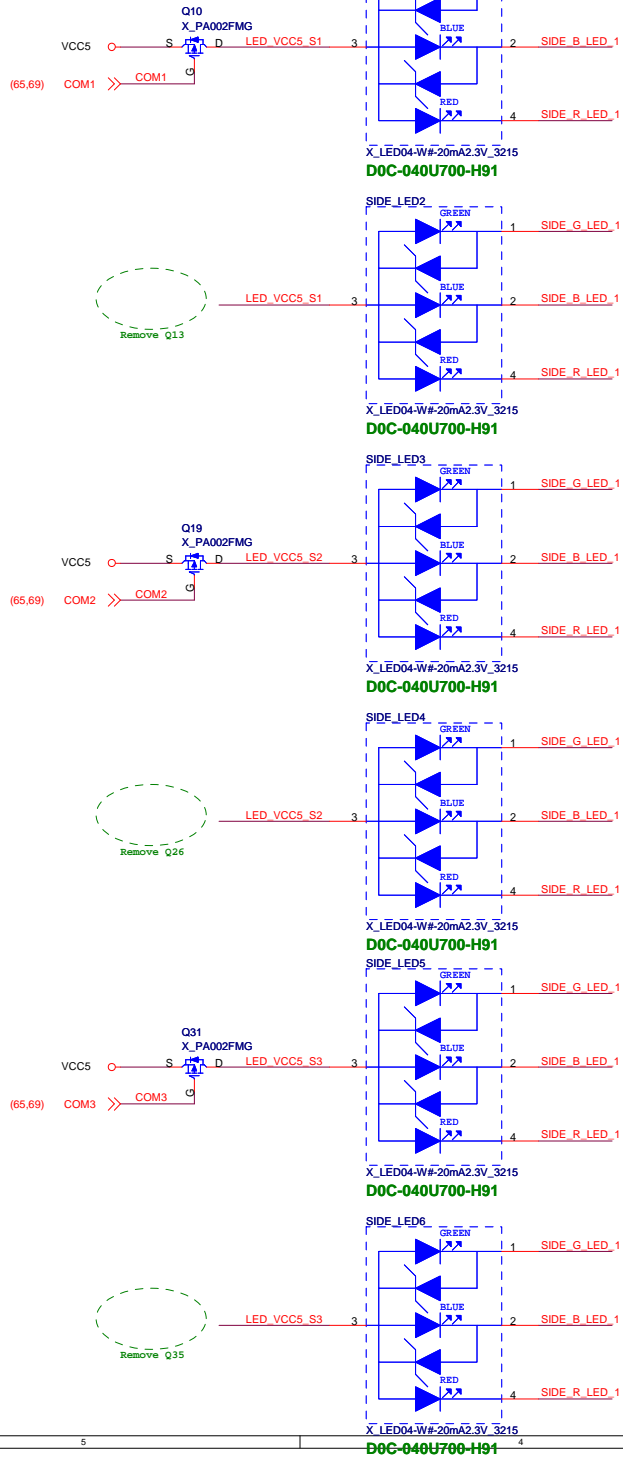
JRAINBOW1JRAINBOW2

JCORSAIR1



MICRO-STAR INT'L CO.,LTD			
MS-7C37			
Size Custom	Document Description LED - JLED1/2/3/4		Rev 3.1
Date: Monday, May 06, 2019		Sheet 67 of 75	

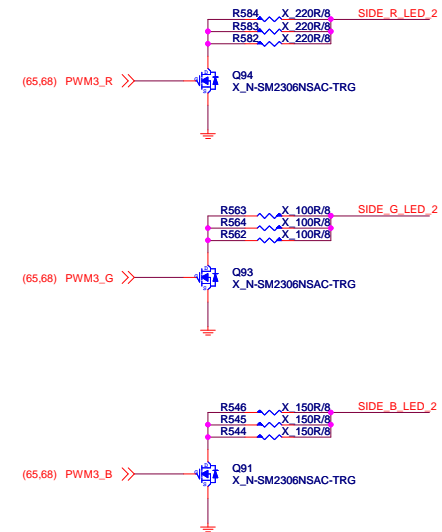
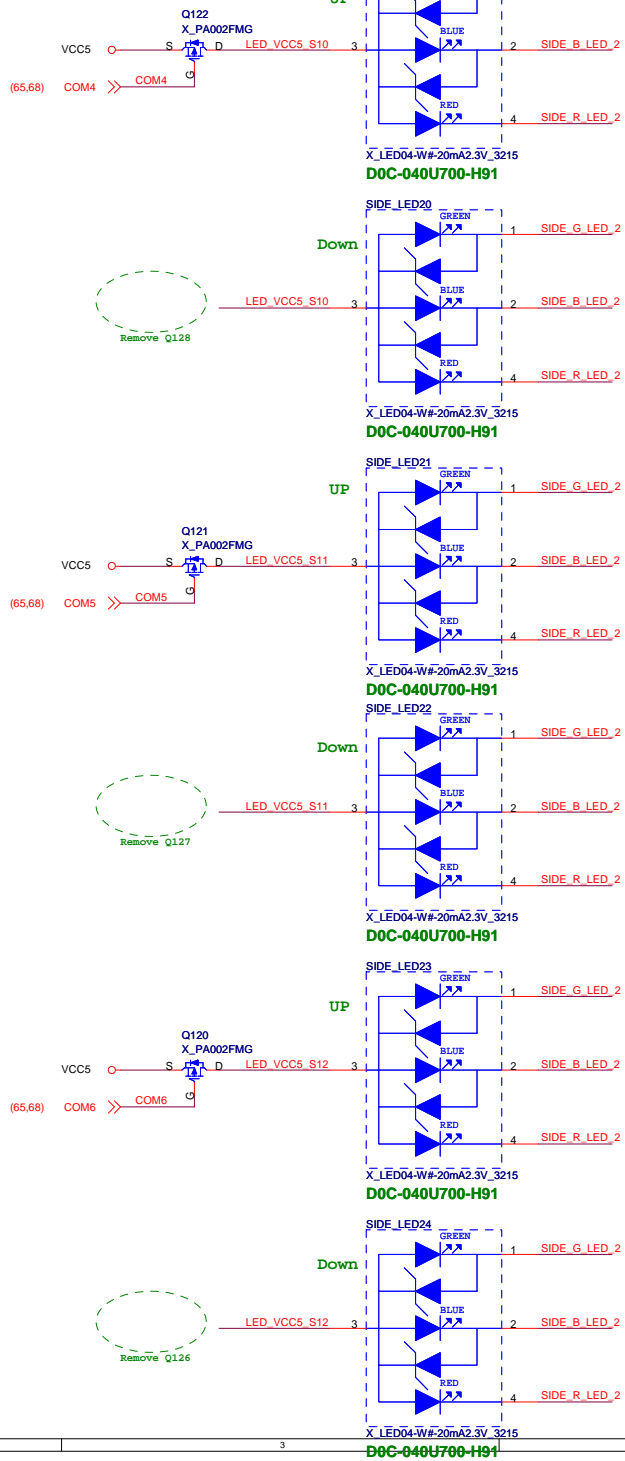
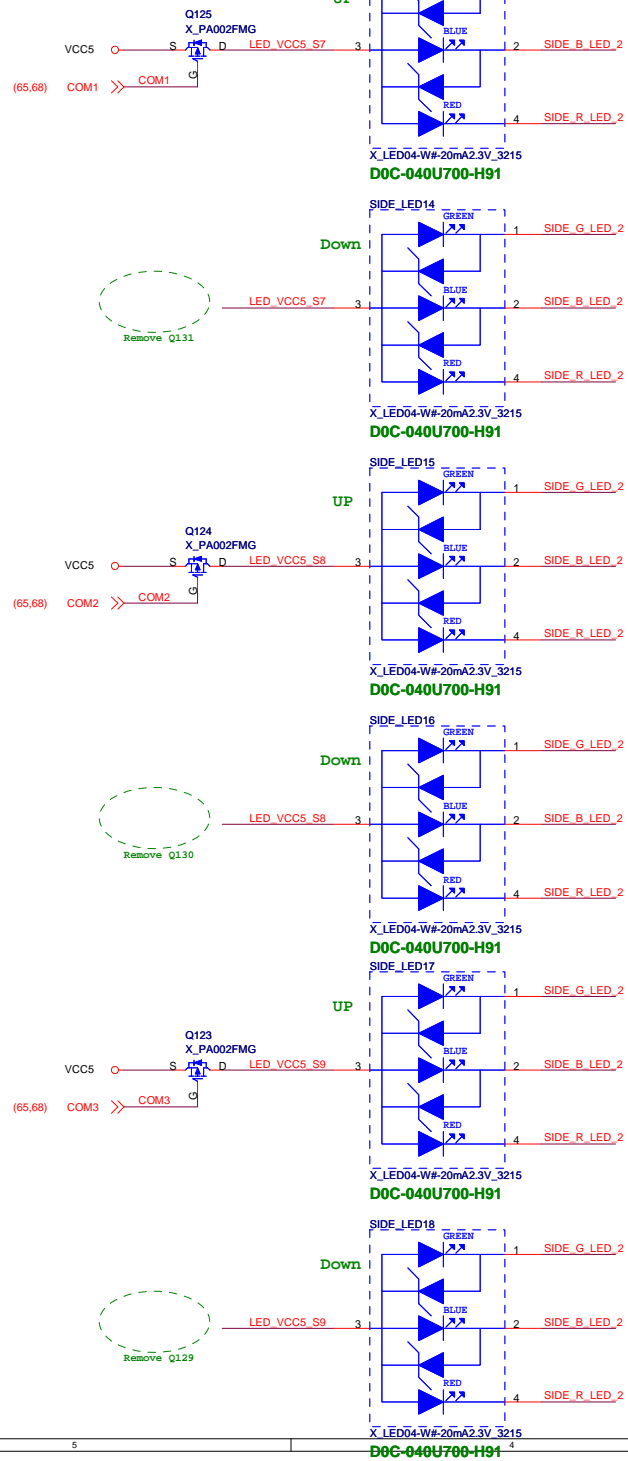
Sidebar LED *12



Vinafix.com

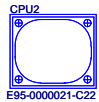
MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size Custom	Document Description	Rev 3.1
LED - Sidebar LED		
Date: Monday, May 06, 2019	Sheet 68	of 75

Market Name LED *12



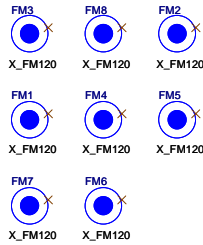
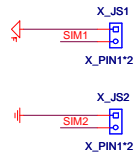
	MICRO-STAR INT'L CO.,LTD		
	MS-7C37		
	Size Custom	Document Description LED - Market Name	Rev 3.1
	Date: Monday, May 06, 2019		Sheet 69 of 75

CPU Socket

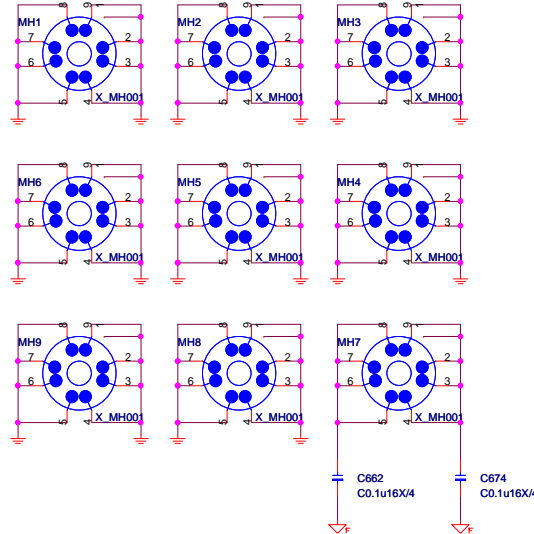


E95-0000022-C22

Simulation



Optics Orientation Holes



MANUAL PART

UEFI1
G51-M1SPXXA-A09
G51-M1SPXXA-A09
HDMI_LA1
Label
HDMI
HDMI LABEL
Y01-RHDMI03-000

MKT_LA1
G51-M1SPP32-Q13
G51-M1SPP32-Q13
NAHIMIC1
Y02-MU00100-NAH
Y02-MU00100-NAH

XSPILT1
X_Y02-MA00401-XSP
Y02-MA00401-XSP
SSE1
X_Y02-MA00101-SSE
Y02-MA00101-SSE

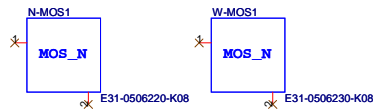
PCB

PCB

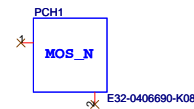


PD0-07C3731-E48

MOS HEATSINK



PCH HEATSINK



Audio COVER



IO COVER

DDR COVER